Design of Two-Rail Checker Using a New Parity Preserving Reversible Logic Gate

Trailokya Nath Sasamal, Ashutosh Kumar Singh, and Anand Mohan

***Abstract*—Reversible logic is one of the basis of future computing system that promises zero energy dissipation. It has applications in various fields such as Low power VLSI, Fault tolerant designs, quantum computing, nanotechnology, DN**

A computing, optical computing, cryptography and informatics. To make reversible logic circuits reliable, they must incorporate fault tolerance attribute. In this paper, we propose a new parity preserving reversible logic gate. We have proposed two optimized design of a self checking two rail checker circuit based on proposed parity preserving reversible logic gate in terms of number of gates and critical path delay. The proposed design achieves less critical delay and gates compared to the existing designs available in literature.

***Index Terms*—Critical delay, fault tolerant, parity-preserving reversible gates, two rail checker.**

I. Introduction

In the current scenario with increasing complexity in VLSI circuits; managing Power dissipation is an important issue Conventional logic circuits dissipate heat in an order of $kTLn2$ joules for every bit of information that is lost, where k is the Boltzmann constant and T is the operating temperature [1]. Information is lost when the input vector cannot be uniquely recovered from its output vectors. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost. It has applications in various domain such as Low power VLSI [2], Fault tolerant designs, quantum computing [3], nanotechnology, DNA computing, optical computing [4], cryptography. According to [5], [6] zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design. Synthesis of reversible logic circuits differs from the conventional one in many ways. Firstly, in reversible circuit there should be no fan-out, that is, each output will be used only once. Secondly, for each input pattern there should be a unique output pattern. Finally, the resulting circuit must be acyclic. Any reversible gate performs the permutation of its input patterns only and realizes the functions that are reversible. If a reversible gate has k inputs, and therefore k outputs, then we call it a $k \times k$ reversible gate. Any reversible circuit design includes only the gates that are reversible. In a reversible circuit, the outputs that are not used as primary outputs are called garbages and the input lines that are set to constants are termed as constant inputs. An efficient design should keep both the number of garbage outputs and constant inputs to minimum.

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of some its components. If the system itself made of fault tolerant components, then the detection and correction of faults become easier and simple. In communication and many other systems, fault tolerance is achieved by parity. Therefore, parity preserving reversible circuits will be the future design trends towards the development of fault tolerant reversible systems in nanotechnology Rand a gating network will be parity preserving if its individual gate is parity preserving [7]. Thus, we need parity preserving reversible logic gates to construct parity preserving reversible circuits. This paper presents a new parity preserving logic gate that is the parity of the inputs matches the parity of the outputs. Such parity-preserving reversible gates, when used with an arbitrary synthesis strategy for reversible logic circuits, allow any fault that affects no more than a single logic signal to be detectable at the circuit's primary outputs [7]. NPPRG is universal in the sense that it can be used to synthesize any arbitrary Boolean function. For various types of error detection codes self-checking checker must embedded with other testable block. We have also presented two optimised fault tolerant reversible two rail checker using proposed new gate.

The paper is organized as follows: In Section II, basic concepts about reversible gates are introduced. Section III proposes the new parity preserving reversible gate and Section IV shows two designs of two rail checker using proposed new gate. The resulting design is compared to previous work in Section V and the paper is concluded in Section VI.

II. Reversible Logic Gates

A. Basic Reversible Gates

There exist many reversible gates in the literature. Among them 2×2 Feynman gate (FG) [8], depicted in Fig. 1(a), 3×3 Peres gate (PG) [9], depicted in Fig. 1(b), 3×3 Toffoli gate (TG) [10], depicted in Fig. 1(c) and 3×3 Fredkin gate (FRG) [11], depicted in Fig. 1(d) have been studied extensively.

B. Parity Preserving Reversible Gates

Parity checking is one of the most widely used, methods for error detection in digital systems. It's most common use

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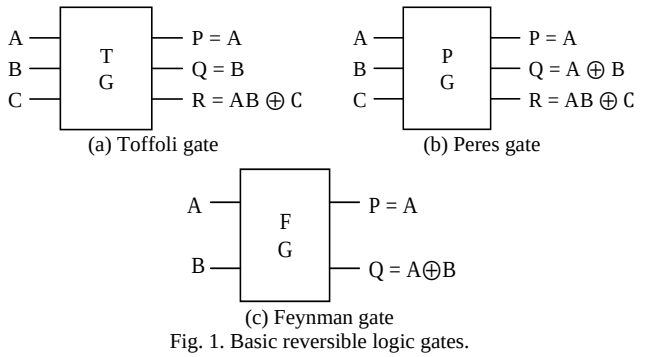
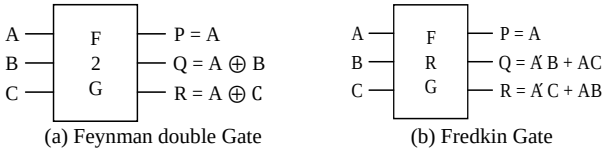
is for detecting errors in the storage or transmission of information, primarily because most arithmetic and other processing functions do not preserve the parity of the data [7]. There have been attempts at performing arithmetic operations on specially encoded operands in a way that parity checking becomes applicable [12], [13]. But the use of traditional methods of error detection in reversible logic, presents some problems, given the requirement for fan-out and the associated increase in "garbage bits", that is, extra bits that are produced to maintain the reversibility property. If computation is performed in such a way that the parity of the input data persists throughout the computation, no intermediate checking would be required. Such results can be forwarded to subsequent modules on the data path, and thus not subject to stringent performance or reversibility requirements. Any erroneous result tends to propagate through the downstream modules without a danger of corrupting additional information in the absence of multiple compensating faults [7]. Given that reversible gates tend to have the same number of input and output lines, a sufficient requirement for parity preservation in the reversible computation, where each gate preserve parity; i.e., have the same parity for input and output lines. More generally, any $k \times k$ reversible logic gate where the EX-OR of the inputs matches the EX-OR of the outputs will be parity preserving. A few parity preserving logic gates have been proposed in the literature. Among them 3×3 Feynman Double gate (F2G) [7] depicted in Fig. 2(a) and 3×3 Fredkin gate (FRG) [11] depicted in Fig. 2(b) are one-through gates, which means one of the inputs is also output. It can be verified from the truth Table I and Table II that the input pattern corresponding to a particular output pattern can be uniquely determined and also satisfying $A \oplus B \oplus C \oplus D = P \oplus Q \oplus R \oplus S$, so parity-preserving feature holds good.



(a) Toffoli gate (b) Peres gate

(c) Feynman gate

Fig. 1. Basic reversible logic gates.



(a) Feynman double Gate (b) Fredkin Gate

Fig. 2. Parity preserving reversible gates.

III. A New Parity Preserving Reversible Gate

This paper presents a new four-input and four-output reversible-logic gate. The truth table of the gate is shown in Table III. From the truth table, it can be verified that the input pattern corresponding to a particular output pattern can be uniquely determined. The new parity preserving reversible gate, NPPRG shown in Fig. 3(a). The corresponding truth table of the gate is shown in Table III. It can be verified from the truth table that the input pattern corresponding to particular output pattern can be uniquely determined. This is readily verified by comparing the input parity $A \oplus B \oplus C \oplus D$ to the output parity $P \oplus Q \oplus R \oplus S$. The newly proposed NPPRG is universal in the sense that it can be used for implementing arbitrary Boolean functions. The implementation of NPPRG gate as AND, OR function, and signal duplication are shown in Fig. 3(b). The NAND, NOR, NOT function, and 1-to-2 decoder can be simultaneously implemented as shown in Fig. 3(c). The EX-OR, EX-NOR functions can be implemented as depicted in Fig. 3(d), and Fig. 3(e) respectively.

TABLE I: Truth Table of the Parity Preserving F2G

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

TABLE II: Truth Table of the Parity Preserving Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

TABLE III: Truth Table of Proposed Universal Fault Tolerant Gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	1
0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	1	1	0	0
0	1	1	0	1	1	1	1
0	1	1	1	0	0	1	0
1	0	0	0	1	0	0	0
1	0	0	1	0	1	0	1
1	0	1	0	0	0	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	0	1
1	1	0	1	0	1	0	0
1	1	1	0	0	1	1	1
1	1	1	1	1	0	1	0

Proposed parity-preserving reversible gate, satisfying

$$A \oplus B \oplus C \oplus D = P \oplus Q \oplus R \oplus S .$$

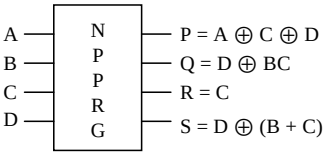


Fig. 3(a). Proposed parity preserving reversible-logic gate.

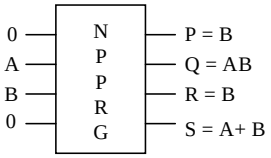


Fig. 3(b). AND, OR, signal duplication.

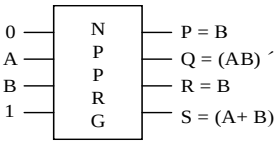


Fig. 3(c). NAND, NOR, NOT, 1-to-2 decoder.

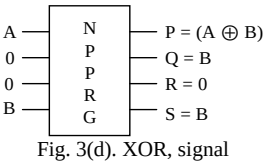


Fig. 3(d). XOR, signal duplication.

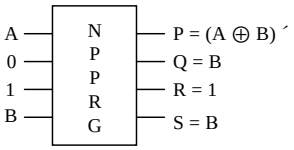


Fig. 3(e). XNOR, NOT, 1-to-2 Decoder.

IV. Design of Two Rail Checker Based on Parity Preserving Reversible Logic Gates

A two rail checker has two groups of inputs (x_1, x_2, x_3,…x_n) and (y_1, y_2, y_3,…y_n) and two outputs e_1 and e_2 .The signals observed on the outputs should always be complementary, i.e. a 1-out-of-2 code if and only if every pair x_i, y_j is also complementary for all $j\,(1 \le j \le n)$.

In a non-error situation when $x_0x_1 = 11, y_0y_1 = 00$; the result of this is $e_1 = 0, e_2 = 1$ valid code (Fig. 4(b)). Now consider a situation where due to fault $y_0y_1 = 10$ output appears 00 or 11 which shows either fault in the checker or at the inputs of the checker. The fault-free checker will produce the complementary outputs if the inputs are complementary. The error checking functions of the two pair rail checker are as follows:

$$e_1 = x_0y_1 + y_0x_1$$
$$e_2 = x_0x_1 + y_0y_1$$

This two rail checker can be cascaded with testable block [14] The outputs q and s of one testable block forms the input x_0 and y_0 for the two-pair rail checker, and the outputs of another testable block forms the input x_1 and y_1 as shown in Fig. 4(a). Thus, the testable blocks are tested using the two-pair rail checker.

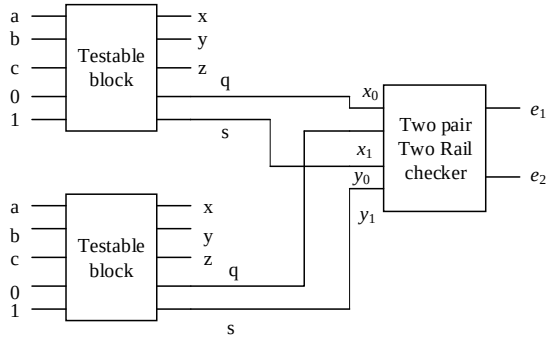


Fig. 4(a). Testable block embedded with the two-pair two-rail checker.

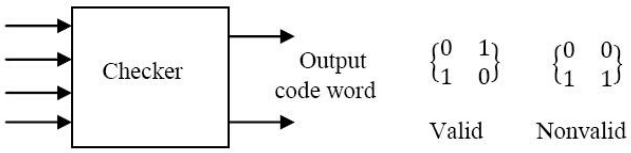


Fig. 4(b). Two rail checker.

Two designs of two-rail checker is constructed using proposed new gate, as shown in Fig. 5 (a), Fig. 6(a). The first design is composed of eight gates i.e. two F2G and six new gates. The second design is realized with six new gates. Existing two-rail checker has been implemented using eight R gates [14].

V. Results and Simulation

A comparison of proposed design with the existing design illustrated in Table V. It shows that the proposed design archives less critical delay as compared with existing design [14]. The proposed parity preserving reversible design 1, design 2 has implemented using 6 and 8 gate respectively, where existing design implemented with 8 gates. The proposed design incorporated with parity preserving feature that enhance fault tolerant attribute, where existing design doesn't have parity preserving feature. The proposed design 2 is more complex but achieves less delay as compared to proposed design 1. All the designs are coded in VHDL for functional verification. The designs are synthesized in Xilinx Virtex-6 FPGA using Xilinx ISE 12.1 for understanding the delay and number of gates [15]. We have created a library of reversible gates in VHDL and used it to code the proposed designs of reversible two rail checker. The functional verification is done using the ISim simulator, which checks the correctness of our proposed designs Fig. 5(b), Fig. 6(b).

TABLE IV: Timing Report

Source Pad	Destination Pad	Path delay*		
		Existing design [15]	Proposed design 1	Proposed design 2
x_0	e_1	5.216	5.270	5.300
x_0	e_2	5.345	5.399	5.368
x_1	e_1	5.262	5.349	5.378
x_1	e_2	5.391	5.477	5.447
y_0	e_1	5.417	5.069	5.099
y_0	e_2	5.546	5.198	5.167
y_1	e_1	5.415	5.415	5.445
y_1	e_2	5.544	5.544	5.513

*All values displayed in nanoseconds (ns).

TABLE V: Comparison of the Proposed Designs with Existing Design

	Existing design[15]	Proposed design 1	Proposed design 2
Parity preserving feature	No	Yes	Yes
Critical delay	5.546 ns	5.544ns	5.513ns
Garbage outputs	8	6	8
No. of gates	10	14	18

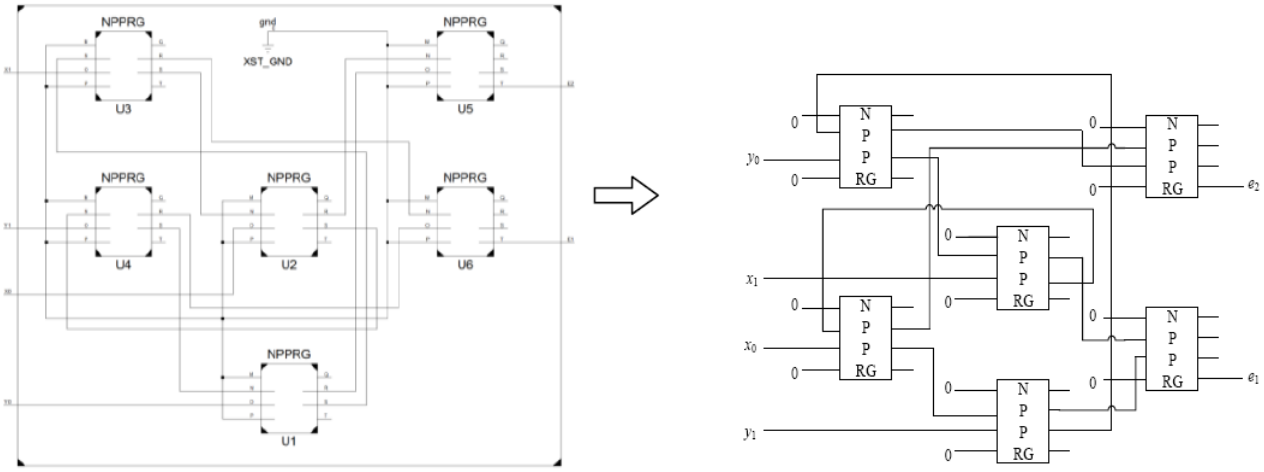


Fig. 5(a). RTL schematic of proposed design 1and proposed design 1.

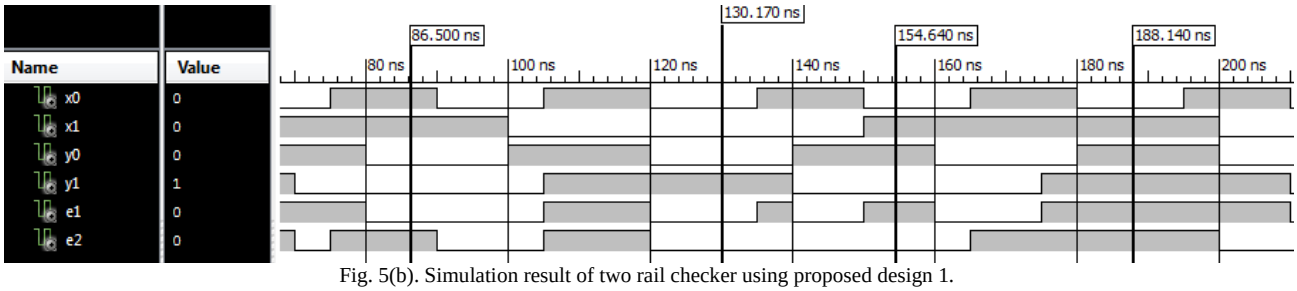


Fig. 5(b). Simulation result of two rail checker using proposed design 1.

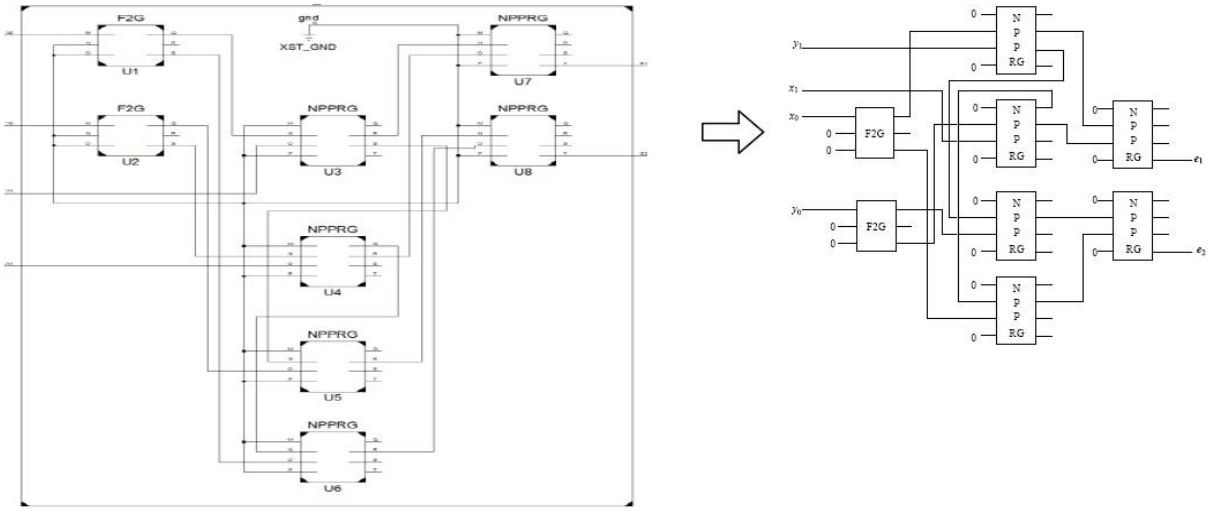


Fig. 6(a). RTL schematic of proposed design 2 and proposed design 2.

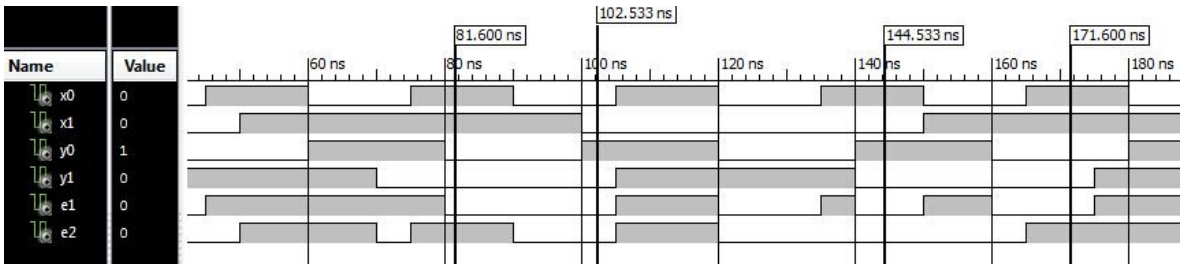


Fig. 6(b). Simulation result of two rail checker using proposed design 2.

VI. Conclusion

A new reversible parity preserving logic gate has been proposed in this paper and presents its universality by implementing all possible Boolean functions. We also presented two designs of reversible fault tolerant two rail checker using the new parity preserving gate with modest hardware overhead. The proposed designs has constructed with the optimum gates and critical path delay. All the designs are functionally verified using VHDL and synthesized using Xilinx Virtex-6 FPGA. The comparative results proved that the proposed designs perform better than

the existing design. Proposed reversible checker can be incorporated with various systems to facilitate online error detection. The reduction of garbage outputs using best synthesis algorithm is the primary concern in reversible gate-based design than the actual number of gates for the designers and currently in progress.

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