Low Power Circuit Design Techniques: A Survey

Nikhil Raj, Ashutosh Kumar Singh, and Anil Kumar Gupta

***Abstract*—This paper presents a detail on various techniques to realize low voltage low power circuit. The techniques discussed are conventional gate-driven (GD), floating gate (FG), quasi-floating gate (QFG), bulk-driven (BD), and BD-QFG. The comparative analysis results in best performance achieved by BD-QFG approach. As BD circuits are well known approach for low power design, the combined effect QFG in bulk driven circuit results in enhanced performance. The complete analysis has been carried out in industry specific node UMC 0.18 micron technology with the help of HSpice simulator.**

***Index Terms*—Quasi-floating gate, bulk-driven, bandwidth, power.**

I. Introduction

Low power and efficient portable equipments demands are rising in day-to-day life. Moreover, a large number of research articles can be found to meet these goals specially when talking about medical equipments. The common trend for analyzing low power circuits is the lowering of supply voltage [1]. But the threshold voltage of metal-oxide-semiconductor (MOS) transistor acts as a main obstacle in lowering of voltage supply after certain limit. The supply must be at least equal to or greater than the threshold of MOS transistors used in circuit realization. The rapid scaling of CMOS processes in nanometer demand low supply which helped digital circuit realization at very low power consumption but it is not true for analog circuit realization. The associated drawback is short channel effect which results in offset, low gain stages, decreased impedance etc. Configuring, the whole system both digital and analog on single chip requires different levels of biasing currents which is fulfilled via current mirrors. To design efficient current mirror with standard gate driven MOSFET that to at low power supply is not possible. To overcome several non-conventional methods like level shifter, sub-threshold, FG, QFG, bulk has been proposed [2].

Every technique has its advantage and disadvantages. Among all, the bulk driven MOS transistors are encouraged for realizing the low power circuits. In bulk-driven MOS transistors, the gate terminal is biased by dc potential to turn on the MOSFET whereas the signal is applied between the bulk and the source of the MOS transistor and causes the drain-to-source current flow. The problems associated with bulk as processing input is its lower transconductance and moreover, requires a twin-well process for fabrication. The effect of decreased transconductance is visible by poor open-loop gain and hence the unity-gain bandwidth. In this respect, the most find suitable approach which is gaining interest nowadays is the combined effect of bulk with QFG MOS transistors. The approach is named as BD-QFG technique [3]. This approach not only work well at low supply but do not require increased the chip area as like FGMOS and QFGMOS.

The objective of this paper is on emphasizing the interest to use BD-QFG transistors which results in enhanced small signal parameter for analog circuit realization. The advantage of the technique is exploited by comparing it with different low power techniques through an example of common source amplifier. Further, a current mirror is also proposed. The HSpice results confirm the BD-QFG to be a better option for low power application. The paper is organized as follows: Section II of the paper covers the summary of low power techniques. Section III comprises the current mirror realization using techniques detailed in Section II. The simulation results in HSpice on 0.18 μm technology are detailed in Section IV. Section V concludes the conclusion of paper.

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II. Low Power Techniques

A. Floating Gate (FG) and Quasi-Floating Gate (QFG)

FGMOS and QFGMOS [4] based circuits can operate at much lower supply. The advantage of these approaches lies in terms of linearity as the input coupling capacitor divider makes input signal to attenuate and increases the linearity. The architecture of N-channel FGMOS (M1) is shown in fig. 1 (a). Under DC analysis, the gate of M1 is at floating potential. The input capacitance is formed by second layer of ploy silicon over the poly layer of gate. The input capacitor (C) formed is named as poly-poly layer (PIP) capacitor. Using the law of charge conservation at floating gate (V_{FG}), the floating gate voltage is given as

$$V_{FG} = \frac{1}{C_T}\left(CV_{IN} + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B + Q_0\right) \qquad (1)$$

where $C_T = C + C_{GS} + C_{GD} + C_{GB}$, C_{GS}, C_{GD}, C_{GB} are the parasitic capacitance associated the floating gate node, and Q_0 is the initial charge trapped in the floating gate during fabrication. The trapped charge Q_0 at floating gate [5] and attenuation of effective gate input voltage due to input capacitor divider were the main obstacles with FGMOS. Many research articles came to overcome these issues at the expense of extra circuitry. Later, with introduction of QFGMOS (architecture similar to FGMOS) associated drawbacks of FGMOS were no more issues. The schematic of QFGMOS (M1) is shown in Fig. 1 (b). The only difference

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lies in converting of floating gate in quasi mode by employing a large valued resistor R_{large} realized by reverse biased junction of P-type MOS transistor (MP) operating in cut-off region. The effective quasi floating gate voltage under ac input in s-domain is expressed as

$$V_{QFG} = \frac{sR_{large}}{1+sR_{large}C_T^{'}}\left(CV_{IN} + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B + Q_0\right) \quad (2)$$

where $C_T^{'} = C + C_{GS} + C_{GD} + C_{GB} + C_{GD}^{'}$ is the total capacitance and $C_{GD}^{'}$ is the parasitic capacitance of transistor working in cut-off region attached to QFG node. The equation (2) represents a high pass filter with its cut-off frequency given by $1/2\pi R_{large}C_T^{'}$. By selection of proper R_{large}, the cut-off frequency can be made very low (even less than 1 Hz) mostly required by bio-amplifiers [6]. So, it can perform as weighted average of ac input voltages from very low frequency to high frequency without affecting the required results till it remains large enough. The only related issue left with these FG and QFG approach was lower transconductance and transient frequency compared to conventional GD approach. Moreover, with these architectures the DC convergence has been a continuously encountered problem by currently available spice simulators.

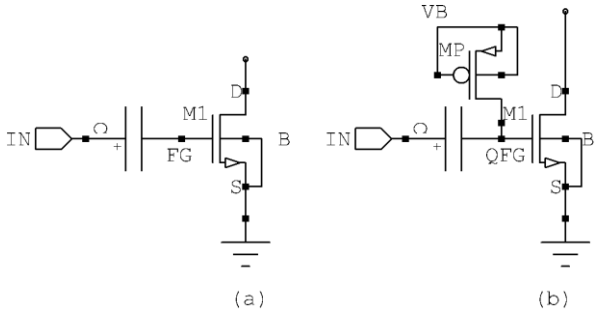

Fig. 1. N-channel: (a) FG, and (b) QFG MOS transistor.

Several FG based applications can be found out of which few are related to design of multiplier, transconductor, filter, I-V converter, CM with wide dynamic range and enhanced bandwidth and many other concerned to low voltage applications such as CM with enhanced bandwidth [7], CM with enhanced characteristics [8]. Taking advantage of capacitor divider property, some QFG based transistors were used for design of very linear programmable CMOS OTA [9] which further used to implement tunable MOS resistors [10] and also GM-C filter [11]. Other recent published articles are based on current conveyor [12], CM having low input compliance voltage [13]. The experimental verification of QFG based circuits in literature proved to be a better technique for realizing low voltage power circuits.

B. Bulk-Driven (BD)

The conventional MOS transistor is a four terminal device whose fourth terminal, the bulk is usually connected either negative/positive supply for N-channel/P-channel transistor, respectively, or to their source terminal. But by using the bulk-terminal as a signal input instead of connecting it to any of the supply voltages or source terminal, the threshold voltage limitation can be removed. Based on this, BD technique was first reported in [14]. The operation is similar to operation of a junction field effect transistor (JFET). The most significant issue related to the bulk-driven is its small body transconductance (g_{mb}) and transient frequency (f_T). The relation of g_{mb} with gate transconductance (g_m) is given as

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f - V_{SB}}} g_m = \eta g_m \quad (3)$$

where γ is the body effect co-efficient, ϕ_f is the Fermi-potential, V_{SB} is the source-to-bulk potential. The normal range of η varies from 0.2 to 0.4. Since, the BD is much sensitive to device mismatch and process variation, positive feedback increases the chances of stability issues at input. Moreover, increased impedance by loop gain affects the non-dominant pole thereby degrading the frequency response of amplifier. A numerous circuits based on this technique targeted to achieve low power can be found. Few are based on op-amp design [15], high gain op-amp [16], highly linear OTA [17] etc.

C. Bulk-Driven Quasi-Floating Gate (BD-QFG)

Using the BD together with QFG MOS transistor, enhanced small-signal characteristics like transconductance and bandwidth over separate BD and QFG-based circuits can be achieved. The approach is introduced with the name BD-QFG technique. The latest related research article using this technique can be seen in design of differential difference current conveyor [18]. This technique is helpful for battery-operated portable devices since its bulk-input processing demand maximum supply not more than a BJT junction turn-on potential to prevent latch-up. Under DC analysis it works as simple BD technique whereas for ac analysis it combines the effect of BD and QFG. The resultant is an improved frequency response over GD.

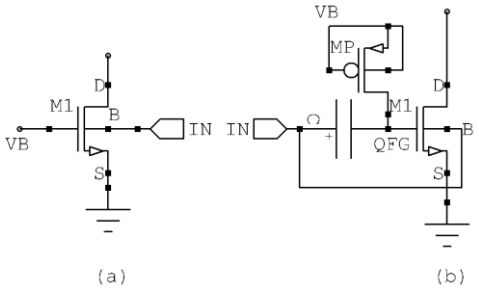

Fig. 2. N-Channel: (a) BD, and (b) BD-QFG MOS transistor.

III. Current Mirror

Current mirror (CM) is a circuit whose function is to copy currents to various blocks in the circuit. A most common example can be found in biasing blocks for operational transconductance amplifier, op-amps, stabilization, current amplification, active loading and level shifting [19]. The design parameters affecting functionality of current mirror are input/output compliances voltage limits, small signal input/output impedances and bandwidth [20]. For supply

below threshold voltage of standard MOS transistors, the conventional current mirror unfit due to its degraded parameters like high input resistance, low output resistance, bandwidth. The analysis of small-signal parameters of current mirror using the discussed low power techniques is shown below (Table I):

TABLE I: COMPARISON OF AFFECT ON PARAMETERS WITH LOW POWER TECHNIQUES

	Threshold	Transcond-uctance	Condu-ctance	Transient frequency
GD	V_{th}	g_m	g_{ds}	f_T
FG	$V_{th,FG} << V_{th}$	$(0.3-0.5)g_m$	$\geq g_{ds}$	$(0.3-0.5)f_T$
QFG	$V_{th,QFG} << V_{th}$	$(0.5-0.6)g_m$	$\geq g_{ds}$	$(0.5-0.6)f_T$
BD	removed	$(0.2-0.4)g_m$	$\leq g_{ds}$	$(0.3-0.5)f_T$
BD-QFG	removed	$(0.7-1)g_m$	$\geq g_{ds}$	$(0.7-0.9)f_T$

A. Gate Driven (GD):

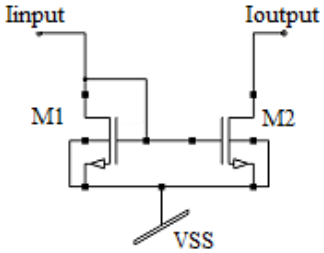

Fig. 3. N-Channel GD current mirror.

Input Resistance, $R_{in,GD} = \dfrac{1}{g_{m1} + g_{ds1}}$

Output Resistance, $R_{out,GD} = g_{ds2}$

Current gain, $A_{I,GD} = \dfrac{g_{m2}/2C_{gs1,2}}{s + g_{m1}/2C_{gs1,2}}$

Dominant pole, $s_{GD} = -\dfrac{g_{m1,2}}{2C_{gs1,2}}$

B. Floating Gate (FG) Driven CM

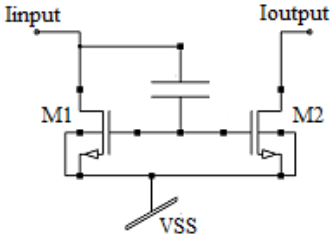

Fig. 4. N-Channel FG current mirror.

Input Resistance, $R_{in,FG} = \dfrac{1}{kg_{m1} + g_{ds1,FG}}$

Output Resistance, $R_{out,FG} = g_{ds2,FG}$

Current gain, $A_{I,FG} = \dfrac{kg_{m2}/(C \parallel 2C_{gs1,2})}{s + kg_{m1}/(C \parallel 2C_{gs1,2})}$

Dominant pole, $s_{FG} = -\dfrac{kg_{m1,2}}{(C \parallel 2C_{gs1,2})}$

where k is the effective capacitance ratio of input to C_T.

C. Quasi-Floating Gate (QFG) Driven CM

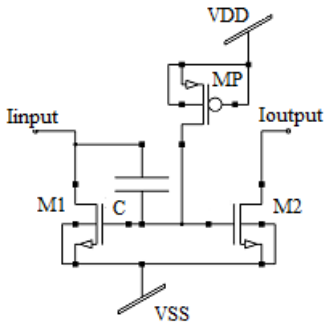

Fig. 5. N-Channel QFG current mirror.

Input Resistance, $R_{in,QFG} = \dfrac{1}{k_1 g_{m1} + g_{ds,QFG}}$

Output Resistance, $R_{out,QFG} = g_{ds2,QFG}$

Current gain, $A_{I,FG} = \dfrac{k_1 g_{m2}/(C \parallel (2C_{gs1,2} + C_{gd,MP}))}{s + k_1 g_{m1}/(C \parallel (2C_{gs1,2} + C_{gd,MP}))}$

Dominant pole, $s_{QFG} = -\dfrac{k_1 g_{m1,2}}{(C \parallel 2C_{gs1,2} + C_{gd,MP})}$

where k_1 is the effective capacitance ratio of input to C_T'.

D. Bulk Driven (BD) CM

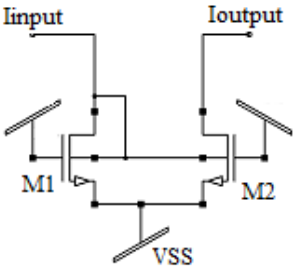

Fig. 6. N-Channel BD current mirror.

Input Resistance, $R_{in,BD} = \dfrac{1}{g_{mb1} + g_{ds1,BD}}$

Output Resistance, $R_{out,BD} = g_{ds2,BD}$

Current gain, $A_{I,FG} = \dfrac{g_{mb2}/2C_{sb1,2}}{s + g_{mb1}/2C_{sb1,2}}$

Dominant pole, $s_{BD} = -\dfrac{g_{mb1,2}}{2C_{sb1,2}}$

E. Bulk Driven Quasi-Floating Gate (BD-QFG) Driven CM

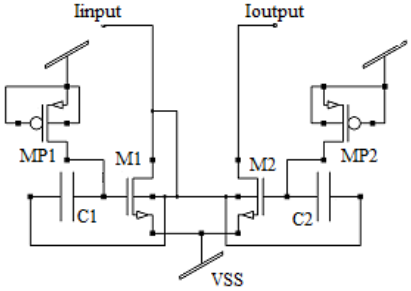

Fig. 7. N-Channel BD-QFG current mirror.

Input Resistance, $R_{in,BD-QFG} = \dfrac{1}{k_1 g_{m1} + g_{mb1} + g_{ds1,BD}}$

Output Resistance, $R_{out,BD-QFG} = g_{ds2,BD}$

Current gain,

$$A_{I,FG} = \frac{(k_1 g_{m2} + g_{mb2})/(C_{1,2} \,||\, (2C_{gs1,2} + 2C_{sb1,2} + C_{gd,MP}))}{s + (kg_{m1} + g_{mb1})/(C_{1,2} \,||\, (2C_{gs1,2} + 2C_{sb1,2} + C_{gd,MP}))}$$

Dominant pole,

$$s_{BD-QFG} = -\frac{k_1 g_{m1,2} + g_{mb1,2}}{C_{1,2} \,||\, (2C_{gs1,2} + 2C_{sb1,2} + C_{gd,MP})}$$

Comparing, the small-signal parameters of the stated techniques it if found that

For input resistance,

$$R_{in,BD-QFG} < R_{in,QFG} < R_{in,GD} \leq R_{in,FG} << R_{in,BD} \quad (4)$$

For output resistance,

$$R_{out,GD} \geq R_{out,QFG} > R_{out,FG} \geq R_{out,\mathrm{BD-QFG}} \approx R_{out,BD} \quad (5)$$

For bandwidth,

$$BW_{BD-QFG} > BW_{QFG} \geq BW_{GD} \geq BW_{FG} >> BW_{BD} \quad (6)$$

From (4), (5) and (6) it can be easily noted that the best condition which is required by ideal current mirror is fulfilled via BD-QFG technique.

IV. Simulation Results

The current mirror is simulated on 0.18 μm mixed-mode twin-well technology provided by UMC with the help of HSPICE simulator. The circuit has been designed with four different LP techniques and compared with the conventional GD current mirror. The W/L ratio of MOS transistors used for design of current mirror is shown in Table II. The values of other parameters assumed for analysis is also listed in Table II.

TABLE II: W/L Ratio of MOS Transistors Used in CM OTA

Transistors	W (μm)	L (μm)
M1	15	0.24
M2	15	0.24
MP1	0.24	0.24
MP2	0.24	0.24
Vdd/Vss= ± 0.3V,C=C1=C2=1pf, Ibias=165uA		

The DC transfer characteristics are shown in Fig. 8. The input current is swept for 150uA. It can be observed that techniques other than bulk-driven perform better in current copying. This is due to non-linear behavior of MOS under bulk as processing input in sub-micron channel length. To suppress the offset current and minimize the non-linear characteristics can be achieved by using an offset current at the output node and use of high dimension MOS device. The input resistance and output resistance plot for current mirror realized under different low power techniques is shown in Fig. 9 and Fig. 10 respectively.

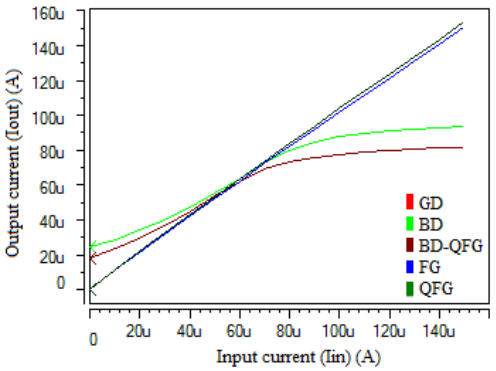

Fig. 8. Comparison of DC transfer characteristics.

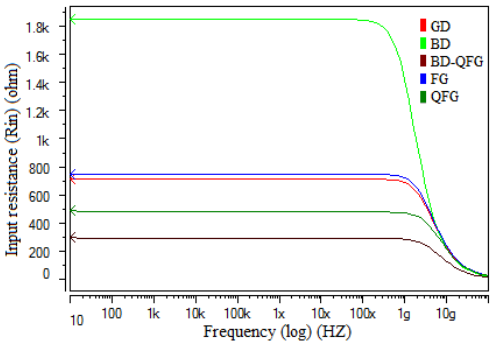

Fig. 9. Comparison of input resistance.

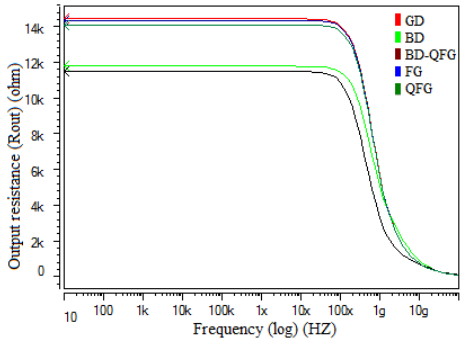

Fig. 10. Comparison of output resistance.

Form the response, the BD-QFG approach proves to be a better option for realizing current mirror. The frequency response shown in Fig. 11 reveals the highest bandwidth achieved by BD-QFG technique.

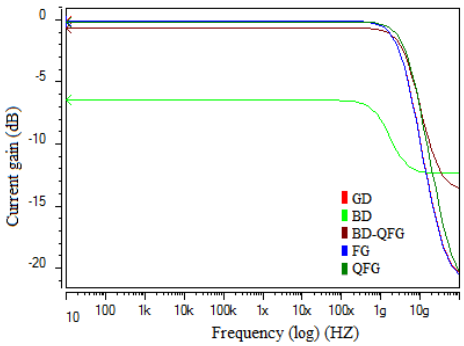

Fig. 11. Comparison of bandwidth.

The comparative analysis effect of all techniques on current mirror is summarized in Table III. It results easily reveals the advantage of BD-QFG not only in terms of parameter enhancement but consumes the low power.

TABLE III: COMPARATIVE ANALYSIS OF PERFORMANCE METRICS OF CM

Technique	Rin (ohm)	Rout (ohm)	Bandwidth (HZ)	Power (μw)
GD	714	14.4k	3.35G	197
FG	749	14.4k	3.21G	197
QFG	481	14.1k	4.64G	197
BD	1.85k	11.8k	1.67G	160
BD-QFG	292	11.5k	5.17G	159

V. CONCLUSION

In this paper, different low power techniques have been discussed. To verify the advantage and disadvantages of such techniques is done with the help of current mirror. Among the discussed approaches, the bulk-mode being a low power option encourages the BD-QFG approach. The enhanced small-signal parameter of current mirror like input/output resistance and bandwidth can be useful for high frequency application. The designs have been implemented using 0.18 μm twin-well process through HSpice simulator.

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