Design of Ethernet-VLC Data Conversion System Based on FPGA

Guiling Sun, Weijian Zhao, Ruobin Wang, and Xuanjie Li

***Abstract*—Visible light communication (VLC) has attracted people's attention due to its wide range of spectrum resources and good privacy in recent year. But research on visible light communication is mostly focused on LED materials, transfer protocol, transmission rates, etc. Lack of research that connect the visible light communications with existing communications methods. In this paper, we propose an Ethernet-visible data conversion system based on FPGA, including Ethernet interface logic, bit-width conversion logic, data buffer logic, and visible light communication transceiver logic. The proposed system achieves Ethernet and visible light access, and realizes 1000Mbps Ethernet data and 625Mbps visible light data conversion. Through buffer control, Ethernet data can be completely and reliably transmitted from high speed to low speed. By defining the structure of visible light communication frame and adding data self-recovery mechanism, data transmission has higher stability on the path of visible light. The feasibility of the system is proved by actual measurements.**

***Index Terms*—Data conversion, ethernet, FPGA, visible light communication.**

I. Introduction

Wireless communication technology is widely used in our lives. As an emerging technology, visible light communication (VLC) is gradually entering the field of academics. Along with the popularization of solid-state lighting, LED (Light Emitting Diode) has been applied to a large area. The Visible Light Communication uses LED as carrier, and uses electromagnetic wave in the visible light band as a carrier to modulate data information onto visible light, thereby achieving communication through it. Most of visible light communication researches focus on the point-to-point transmission in LOS (Line-of-sight) case [1]. Visible Light Communication doesn't occupy scarce radio spectrum and can be used without any license [2].

At present, research on visible light communication mostly focuses on material research [3], coding methods [4], modulation methods [5], and equalization methods [6]. Research focuses more on increasing transmission rates [7]. There are less researches on application. Some researches use visible light as a supplement to RF technology [8]. Some researches on CDMA achieve multi-user access [9]. In the application scenario. Some researches use the visible light communication for audio transmission [10] and video display [11]. And underwater communication is performed with visible light [12]. These researches didn't take advantage of indoor applications of visible light. As an ideal indoor communication, visible light can be combined with common communication. The related research is currently lacking. Ethernet is the most widely used communication technology. Most the rate of visible light communication applications on Ethernet are less then 100Mbps. Based on this, we propose an application design that combines visible light with Gigabit Ethernet. The research can solve the problem from Ethernet to visible light

The Ethernet-VLC data conversion system can achieve bidirectional adaptation of visible light signals and Ethernet signals, thereby accessing the purpose of connecting visible light to Internet. The system uses fluorescent white LED. The modulation method of visible light communication is OOK (on-off keying). The visible light transceiver uses binary code. There is a large gap between the uplink and downlink of the visible light transmission rate at present [13]. The communication bandwidth of fluorescent white LED is lower than Gigabit Ethernet. In system, the communication speed of LED is 625Mbps, which is lower than the speed of Gigabit Ethernet, they cannot be connected directly, and the conversion system are required.

We propose an 1000Mbps Ethernet and 625Mbps visible light communication data conversion system. The system is based on FPGA to realize the transition of data flow. The system ensures the start, progress, and completion of data transmission applications. By defining the structure of visible light communication data frame and combining data stream self-recovery mechanism, the proposed method improves the stability of data transmission.

II. Modules of the System Design

The system is based on Xilinx FPGA Integrated GTP transceivers design. The proposed system block diagram is shown in Fig. 1. In the downlink, the 8-bit wide Gigabit Ethernet data is converted to 32-bit data through the Ethernet interface logic and the bit-width conversion logic. The frame is decelerated in the Ethernet-VLC buffer logic, the visible light communication transceiver logic framing and sent frame to optical path. In the uplink, the GTP transceiver receives the data from the optical path, performs de-frame processing through the transceiver logic, and sends the data to the VLC-Ethernet buffer logic to speed up to Gigabit. And

Manuscript received December 21, 2019; revised March 11, 2020. This research was partially supported by the National Key Research and Development Program of China (2017YFB0403604) and supported by Tianjin Key Laboratory of Optoelectronic Sensor and Sensing Network Technology.

Guiling Sun, Weijian Zhao, and Ruobin Wang are with the College of Electronic Information and Optical Engineering, Nankai University, Tianjin 300350, P.R. China (e-mail: sungl@nankai.edu.cn, zhaoweijian@mail.nankai.edu.cn, wangrb@mail.nankai.edu.cn).

Xuanjie Li is with School of Electronic, Electrical and Communication Engineering, University of Chinese Academy of Sciences, Beijing 100049, P.R. China (e-mail: boylixj@foxmail.com).

then the 8-bit data is restored by the bit-width conversion logic. Finally, the frame is issued via the Ethernet interface.

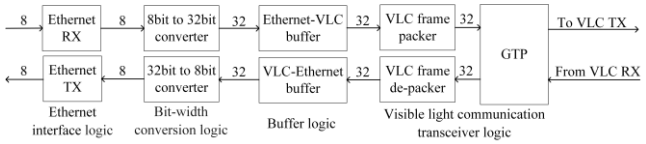


Fig. 1. Ethernet-VLC data conversion system block diagram.

A. Ethernet Interface Logic

The Ethernet interface logic completes the establishment of the communication interface and the configuration of the PHY chip. The functional diagram of the module is shown in Fig. 2. This interface logic design based on RGMII consists of three parts, i.e., SMI (Serial Management Interface), RX, and TX. SMI logic configures the registers in the Ethernet PHY layer slave through the MDC and MDIO interfaces to implement reset and auto-negotiation functions. When the auto-negotiation succeed, Ethernet interface logic will be enabled. RX logic receives the Ethernet data, removes the frame header, and sends data information to bit-width conversion module after performing the CRC (Cyclic Redundancy Check) [14]. TX logic receives data sent from bit width conversion logic for new framing transmission. The frame interval needs to meet the minimum frame interval of the Ethernet in the process of transmission. The minimum frame interval of Gigabit Ethernet is 96 ns, and one clock is configured for 8 ns. When the interval time satisfies 12 clocks, the time is to enable signal. And the previous logic starts to send the package, otherwise the signal will be set low.

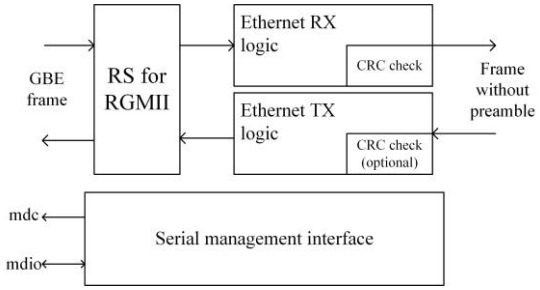


Fig. 2. Ethernet interface logic functional diagram.

B. Bit-width Conversion Logic

Because the design use GTP transceivers which only support 16-bit and 32-bit width data, we should perform width conversion. Considering that high bit width can reduce the frequency of the synchronous clock, this paper use 32-bit width. The bit width conversion logic is based on pseudo-dual-port RAM (Random Access Memory). The downlink writing bit-width is 8, the readout bit-width is 32, the uplink writing bit-width is 32, and the readout bit-width is 8. The uplink and downlink writing and readout operations are similar. Here we take an 8-bit to 32-bit module as an example.

In order to facilitate reading and writing, three address pointers are defined. The pointer WP (write pointer), write data with 8-bit width to RAM in ascending order of address. When writing the last byte of data frame, the first write address of the next frame is determined according to the length of the data frame. When the frame length is a multiple of 4, WP increases normally. When the frame length is not a multiple of 4, WP go to the next address that is a multiple of 4. The pointer RP (read pointer), read 4 bytes of data from high to low at a time. The pointer VP (valid pointer), will be determined if the received data frame check value is correct. If the frame writing into buffer is correctly verified, VP will go to the current position of WP. If the frame writing into buffer is incorrectly verified, WP will be returned to the current VP position.

The maximum byte-length of the Ethernet frame is 1518 and the minimum byte-length is 64. In order to satisfy the requirement of storing one frame of data, the capacity of the RAM is at least 2048 bytes (16384 bits). So the RAM capacity is 16Kb. In order to avoid the conflict when the address is read and written at the same time, the WP will be turned on after the full frame is written completely. However, when the previous frame is reading, the next frame is written completely, e.g. when after the frame A of length 1518 bytes is written, a frame B of length 64 bytes is written. The frame B is written during the reading of the frame A. But at this time, there is no logic to lay in the length information of frame B. Therefore, a FIFO (First Input First Output) storing length information is added to cooperate with the RAM to perform bit-width conversion. Considering that the capacity of the RAM is 2048 bytes, the FIFO bit-width is 11 and the bit-depth of the FIFO is 32 (2048 bytes/64 bytes).

Taking one frame as an example. The frame is written to the RAM according to the writing-enable signal. And then frame checked by CRC. If the result is correct, the signal will be pulled up raised one clock. The length information will be stored into the FIFO and VP go to WP. If the result is error, the writing-enable signal does not pull up, then WP will go to VP. The timing diagram for the writing operation is shown in Fig. 3.

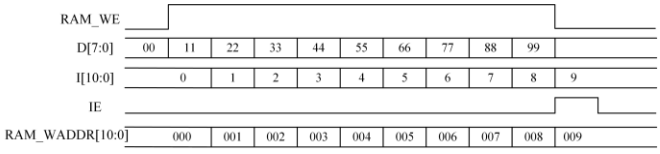


Fig. 3. 8bit to 32bit module write operation timing diagram.

The RAM_WE is the writing-enable signal of RAM. When the signal is enabled. The 8-bit data D [7:0] is written into the RAM with the write address RAM_WADDR [10:0]. In this process, the length information I [10: 0] cached into the FIFO. The signal IE represents a frame is written.

Frame readout based on FIFO status. Detect the status of FIFO. If FIFO is not empty, the reading process of one frame is started and the length information of the current frame is read from the FIFO. The reading timing diagram as shown in Fig. 4.

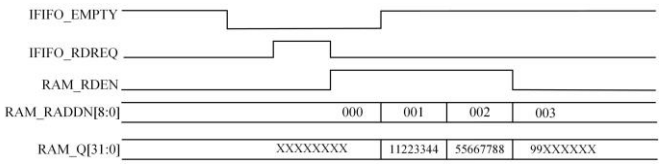


Fig. 4. 8bit to 32bit module readout operation timing diagram.

C. Buffer Logic

The buffer logic is the core of the system. The buffer in the uplink is responsible for slowing down the high-speed Ethernet data frames to the low-speed visible-light clock domain. In the downlink, the frame received from the visible light communication carried to the Ethernet clock domain. Thereby the logic implements two-way communication. The FIFO feature is suitable for buffers, which can reduce the complexity of the design [15]. The uplink and downlink buffers are composed of two asynchronous FIFOs, namely, the DFIFO (Data FIFO) that stores the data frame and the IFIFO (Information FIFO) that stores the frame length information. High-speed data synchronization to low-speed clock is a design difficulty.

The data transmission process complies with the Ethernet TCP/IP protocol. And there is a timeout retransmission rule. After the transmitter sends out one frame, if the acknowledgment information fed back by the receiver is not received within a certain period of time, the transmitter will resend the data until the feedback is received. Because data is transmitted from high speed to low speed and the buffer will be full, discard of data frames is inevitable. But according to this rule, the receiver can receive the complete information correctly through the read-write control. The speed-down buffer is implemented based on this rule.

Depth calculation is very important to pass the data between different clock domains [16]. In downlink the deeper FIFO depth is better to use in speed-down buffer. Considering the device performance, the DFIFO bit-depth used in this paper is 8192 and the bit-width is 32. To better control the buffer capacity, the threshold is set in the buffer. The amount of DFIFO (dfifo_data_count) is maintained between upper threshold and lower threshold. The longest frame has a byte-length of 1518, and a bit-depth of 190 in buffer. The shortest frame has a byte-length of 64, and a bit-depth of 190 in buffer. Considering the situation of continuously writing the longest frame, the upper threshold should ensure that the buffer is not full. The upper threshold is set to 7811 (8191-190*2). The lower threshold keeps FIFO at half full state, and is set to 3715 (4095-190*2). In uplink, the data pass through the buffer from low speed to high speed. There is no data congestion. When the back-to-back transmission is satisfied, two 1518-byte frames are continuously received. Since the FIFO depth is 2^n, it takes 4096 bytes and the bit-width is 32, so the bit-depth is 1024. The speed-up buffer IFIFO may approach the full state due to a large number of 64-byte frames are written. To avoid the IFIFO being full, upper threshold is set to 495 (511-8*2), and the lower threshold is set to 8.

The writing process flowchart is shown in Fig. 5. When the dfifo_data_count surpass the upper threshold, the writing-enable signal is turned off to stop writing. At this time, the buffer is only readout enabled. When the dfifo_data_count falls to the lower threshold, the writing-enable signal is enabled to continue writing data.

The data readout process is shown in Fig. 6. When the data in the IFIFO is not empty, the length information will be read, and the data frame will be read according to data length. If IFIFO is empty and DFIFO is non-empty, it indicates that data fragments exist in DFIFO. Currently, stop writing to clear FIFO, and rely on this fragment cleaning mechanism to ensure the integrity of data transmission.

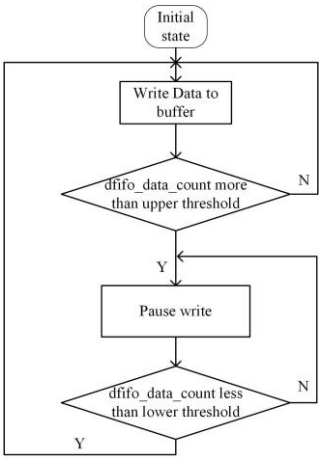


Fig. 5. Buffer write control flowchart.

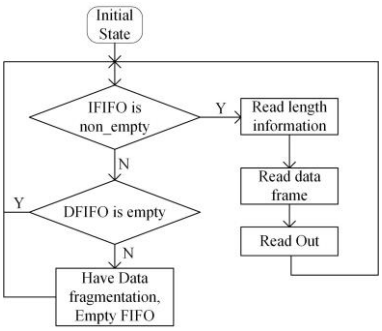


Fig. 6. Frame readout process in buffer.

D. Visible Light Communication Transceiver Logic

The visible light communication transceiver logic assembles the data information into an VLC frame and sends it to the visible light channel via FPGA integrated GTP transceiver. The data clock recovery is integrated inside the GTP transceiver receiver. The data frame structure used in this paper is shown in Fig. 7. The data frame is based on 8B/10B coding technology. High-speed data transmission or data bus often uses 8B/10B protocol [17]. The visible light communication uses OOK modulation. The 8B/10B coding has a level-balancing feature that ensures that the LED does not flicker. The 8B/10B encoded data is serialized and deserialized via GTP transceiver. The frame includes a frame synchronization code, a frame start delimiter, a frame load, and a frame check. After the bit-width conversion, the frame bit-width is 32, that is, 4 bytes of data are processed under the same clock edge. For each frame, a frame synchronization code (0xff0000bc) is sent, which marks the arrival of a frame. Frame start delimiter (0xffxxxxfb) contains the length information of the frame (xxxx is the length information), and the length range is from 0 to 65535. Then the frame load is sent, that is, the encapsulated frame carries the data information. A frame check is added after the data part is over, which is used by the receiver to check, filter, and remove the data frames that have errors during transmission. The frame check in solution uses CRC32. The calculation starts from the frame start code and stops at the end of the data part. There is a frame interval between data frames, where 0xbc is sent, corresponding to K28D5 of 8B10B. When the transmission

is idle, the transmitter will continuously send K28D5, which provides the receiver with the function of calibration.

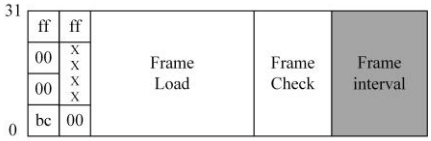


Fig. 7. Visible light communication frame structure.

The overall change process of the frame in the system is shown in the Fig. 8.

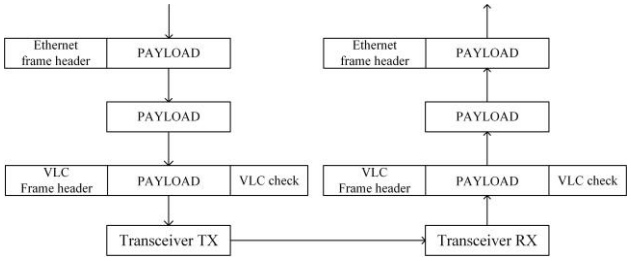


Fig. 8. The change process of frame in system.

The optical path can be easily affected by external interference which results in transmission interrupting. When the optical path is cut off, the receiver will detect a data error. But the transmitter still sent the data, so the data transmission is maintained. At this time, if the optical path is turned on again, the receiver may receive the frame from the middle position, and the communication may be break. In this case, a recovery mechanism is added to the transceiver logic. The receiver must check each frame to be received by the transceiver, and mark the wrong frame. When transmitting to the subsequent logic, the frame will be masked. Normal data transmission is resumed when reconnected.

III. Simulation And Experiment Result

First, the feasibility of the system design is verified through simulation. In the simulation, the transmitter and the receiver of the optical path are connected. Fig. 9 and Fig. 10 are the simulation diagrams of the Ethernet side transmitter and receiver. It can be seen that the data is looped back and the result is correct.

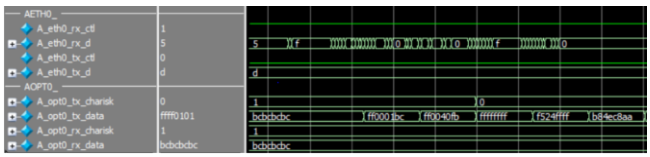


Fig. 9. The simulation diagrams of transmitter.

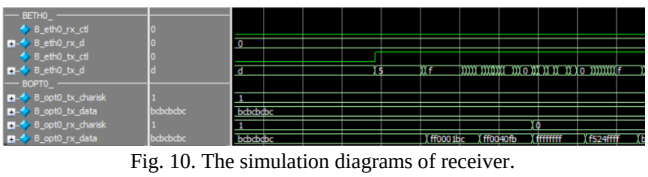


Fig. 10. The simulation diagrams of receiver.

In the system experiment, the VLC side interface is connected to the oscilloscope, and the other side is connected to the Ethernet. The waveform can be observed by the oscilloscope, as shown in Fig. 11. It is verified that the system reaches the rate of 625Mbps.

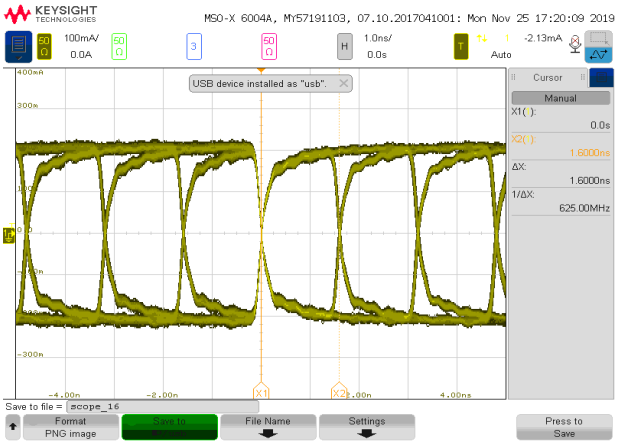


Fig. 11. VLC interface waveform diagram.

In the functional experiment, since the network cannot reach the full-speed Gigabit network in the general environment, a Gigabit Ethernet packet generator is used for the experiment. The packet generator can send data frames with a byte length of 64 to 1518 at full speed. The test environment diagram is shown in Fig. 12. The packet generator sends data to System 1. After the data is converted, it is sent to the System 2 by VLC. After System 2 receives the data, it returns data back to Ethernet and sends it to PC. PC uses the traffic monitoring software NerPerSec to detect the network speed. The network speed is shown in Fig. 13. The transmission rate is close to 500Mbps. Because the system uses 8B/10B encoding and decoding, the ratio between the data rate on the optical path after encoding and the data rate on Ethernet before encoding should be 5: 4. The 625Mbps rate on optical path corresponds to the 500Mbps Ethernet rate. After the optical path is cut and reconnected, the system has restored the data connection, as shown in Fig. 14.

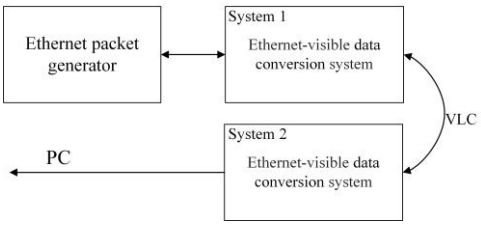


Fig. 12. Test environment diagram.

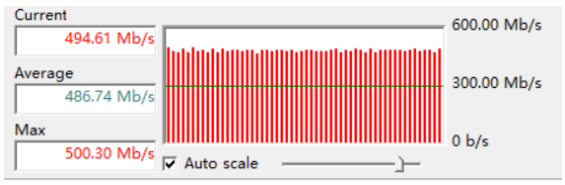


Fig. 13. The Internet speed detected by PC.

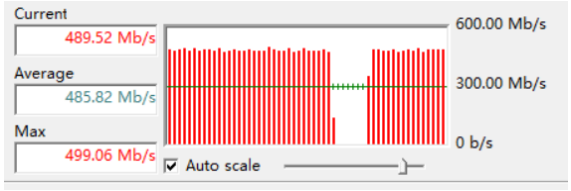


Fig. 14. Effect of self-recovery mechanism.

IV. Conclusion

In this paper, we propose a design of an Ethernet-VLC data conversion system, which can realize the conversion between Gigabit network and 625Mbps optical data. We define the structure of the system and the functions of each module. Through simulation and experiments, we proved the feasibility of the system. And in order to improve the stability of the system, we defined the data frame structure and added recovery system at the receiver. Next, further research will be conducted in the areas of system buffer control and multi-user.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Guiling Sun, Weijian Zhao and Ruobin Wang conducted the research; Guiling Sun and Weijian Zhao wrote the paper; Weijian Zhao and Xuanjie li conducted the design and experiment of test environment; all authors had approved the final version.

References

[1] H. Burchardt, N. Serafimovski, D. Tsonev, S. Videv, and H. Haas, "VLC: Beyond pointto-point communication," *IEEE Commun. Mag.*, vol. 52, no. 7, pp. 98–105, Jul. 2014.

[2] K. Ruediger, "Modulation concepts for visible light communication using video displays," presented at the 2015 IEEE 5th International Conference on Consumer Electronics - Berlin (ICCE-Berlin), Berlin, Germany, Sept. 6-9, 2015.

[3] X. Liu *et al*., "An InGaN micro-LED based photodetector array for high-speed parallel visible light communication," presented at the 2018 Asia Communications and Photonics Conference (ACP), Hangzhou, China, Oct. 26-28, 2018.

[4] K. Sekhar and R. Mitra, "Performance analysis of DCO-OFDM over precoded massive MIMO VLC channel," presented at the 12th IEEE International Conference on Advanced Networks and Telecommunications Systems (ANTS), Indore, India, Dec. 16-19, 2018.

[5] H. Li *et al*., "High speed visible light communications based on RGB laser diodes and OOK-NRZ modulation," presented at the Asia Communications and Photonics Conference (ACP), Guangzhou, China. Nov. 10-13, 2017

[6] Y. Wang *et al*., "8-Gb/s RGBY LED-based WDM VLC system employing high-order CAP Modulation and hybrid post equalizer," *IEEE Photonics Journal*, vol. 7, no. 5, pp. 1-7, Dec. 2015.

[7] G. Cossu *et al*., "5.6 Gbit/s downlink and 1.5 Gbit/s uplink optical wireless transmission at indoor distances (≥ 1.5 m)," presented at the 2014 The European Conference on Optical Communication, Cannes, France, Sept. 21-25, 2014.

[8] D. Basnayaka and H. Hass, "Hybrid RF and VLC systems: Improving user data rate performance of VLC systems," presented at the 81st IEEE Vehicular Technology Conference (ATC), Glasgow, UK, May 11-14, 2015.

[9] D. Chen *et al*., "A CDMA system implementation with dimming control for visible light communication," *Optics Communications*, vol. 412, pp. 172-177, Apr. 2018.

[10] Z. Liu, "Design and achievement of the visible light audio communication system," presented at the 2016 IEEE Advanced Information Management, Communicates, Electronic and Automation Control Conference (IMCEC), Xi'an, China, Oct. 3-5, 2016.

[11] J. Xu *et al*., "Transmitter design and synchronization concepts for DaViD display camera communication," presented at the 2019 28th Wireless and Optical Communications Conference (WOCC), Beijing, China, May 9-10, 2019.

[12] G. Cossu *et al*., "Sea-trial of an ethernet-based underwater VLC communication system," presented at the 2018 Optical Fiber Communications Conference and Exposition (OFC), San Diego, CA, USA, Mar. 11-15, 2018.

[13] Y. Wang and C. Nan, "High-speed bi-directional visible light communication system based on RGB-LED," *China Communications*, vol. 11, no. 3, pp. 40-44, Mar. 2014.

[14] M. Abdulnabi and H. Ahmed, "Design of efficient cyclic redundancy check-32 using FPGA," presented at the 2018 International Conference on Computer, Control, Electrical, and Electronics Engineering (ICCCEEE), Khartoum, Sudan, Aug. 12-14, 2018.

[15] Adl and S. Taghi, "A high performance dual clock elastic FIFO network interface for GALS NoC," *Microelectronics Journal*, vol. 76, pp. 69-80, Jun. 2018.

[16] R. Kamal and J. M. Arostegui, "Design of a dynamic depth high-throughput multi-clock FIFO for the DSPIN," presented at the 2015 1st International Conference on Next Generation Computing Technologies (NGCT), Dehradun, India, Sept. 4-5, 2015.

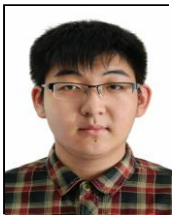
[17] S. Liu, H. Lin, and C. Wang, "The implementation of high-speed data transmission for 8B/10B protocol on FPGAs," presented at the International Conference on Applied System Innovation, Sapporo, Japan, May 13-17, 2017.

Guiling Sun received the Ph.D. degree from Nankai University, in 2004.

She was a professor with Nankai University. She is also the vice director of the Tianjin Institute of Communications, the vice director of the EDA Technology Research Society, North China, and the leader of electronic technology experiment and practice teaching team of Tianjin City.

Prof. Sun has published more than 80 papers and two research monographs in a number of areas about the wireless sensor networks, the Internet of Things, compressed sensing, information detection, and intelligent control systems and signal processing.

Weijian Zhao was born in Tianjin, China in 1994. He received the B.S. degree in microelectronics science and engineering from Nankai University, Tianjin, China in 2017, where he is currently pursuing the M.S. degree in information and communication engineering with the College of Electronic Information and Optical Engineering. His research interests are intelligent control systems and signal processing.



Ruobin Wang was born in Tianjin, China in 1996. He received the B.S. degree in microelectronics science and engineering from Nankai University, Tianjin, China in 2018, where he is currently pursuing the M.S. degree in information and communication engineering with the College of Electronic Information and Optical Engineering. His research interests are information detection and intelligent control systems.

Xuanjie Li received the B.S. degree in electronic engineering from Nanjing University of Posts and Telecommunications, Nanjing, China, 2015. He is pursuing the Ph.D. degree with the School of Electronic, Electrical and Communication Engineering, University of Chinese Academy of Sciences. His research interests are wireless communications.