# Investigation of a Novel High-Permittivity Trench MOS Device with Small Figures of Merit

Junhong Li and Kun Xiao

***Abstract*—We propose a vertical high-permittivity trench power metal oxide semiconductor (HKTMOS) device with an alternating N&P drift regions and high-permittivity (HK) trench sandwiched in between. The unique structure guarantees uniform potential distribution for a wide voltage range at the blocking state owing to both the HK potential modulation effect and the superjunction (SJ) charge balance. The specific on-resistance ($R_{ons}$) of HKTMOS is orders of magnitude lower than the SJ counterparts in the on-state because of the strong accumulation effect brought by the HK trenches. Although the gate charges also significantly rise because of the accumulation, the figures of merit (FOM) of HKTMOS still decrease considerably compared to the SJ under the same device length condition. An expression for the FOM is derived, demonstrating that the FOM of HKTMOS is proportional to the square of the HK trench depth, which agrees with the simulation results well. The simulation indicates that within the BV range of 500~2000 V, the $R_{ons}$ of HKTMOS is 1~2 orders of magnitude lower than that of SJ, and its FOM is 17.4%~44.1% that of SJ under the same device size condition. Furthermore, HKTMOS also demonstrates better charge imbalance tolerance than SJ.**

***Index Terms*—High permittivity, figures of merit, specific on resistance, power MOS.**

## I. Introduction

The performance of silicon power devices is essential for energy conversion systems. To achieve better efficiency, significant efforts have been devoted to the optimization of the breakdown voltage (BV), on-resistance ($R_{on}$) and switching speed of the power device. The current benchmark for power MOS devices is the Super Junction device (SJ) [1]-[4], which is the target and standard for subsequent novel devices. Although several studies have claimed that the device they have proposed has broken the silicon limit created by SJ, these devices have only worked better than SJ for a subset of the features or under specific conditions. For example, the device proposed in [5] indeed enjoyed better specific-$R_{on}$ ($R_{ons}$) than the SJ with given BV. However, as the accumulation effect is used with $SiO_2$ dielectric, the device in [5] suffers much more switching loss than the SJ, the performance comparison with SJ therefore did not make sense if the switching loss is ignored.

Manuscript received December 18, 2017; revised February 23, 2018. This work was supported by the National Natural Science Foundation of China under grant 61204084.

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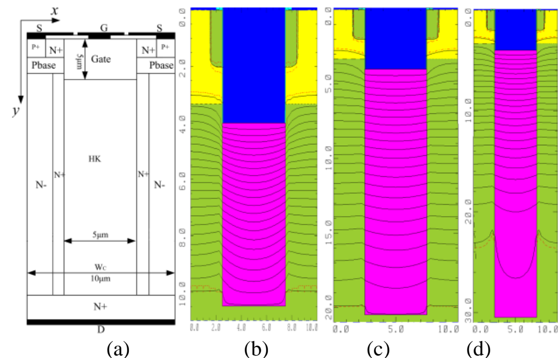



Fig. 1. The re-drawing of the device in [12] with N- drift region doping of $10^{15}$ cm$^{-3}$, N+ sidewall doping of $1\times10^{18}$ cm$^{-3}$, Pbase doping of $3\times10^{16}$ cm$^{-3}$, P+, N+ doping of $10^{20}$ cm$^{-3}$ (a) and its the potential distribution, for the device lengths of 10 μm (b), 20 μm (c), and 30 μm (d), respectively. The drain voltage are 120 V, 240 V, 480 V, and the potential difference between equipotential lines are 5 V, 10 V, 20 V, respectively.

However, we believe that high permittivity (HK) material is the potential solution for further promotion of the silicon limit after SJ. According to [6]-[8], if the silicon junctions are interleaved with dielectric, the reverse BV of the PN junction will be boosted because the dielectric assists in the depletion of silicon. The BV will be improved even using low-permittivity dielectric material, such as poly silicon or $SiO_2$ [6]-[8]. If the $SiO_2$ is replaced by HK material, with its high permittivity, the assistance for depletion will be much stronger; therefore, much better potential distribution and higher device breakdown voltage (BV) will be achieved [9]. The effect is referred to as HK potential modulation (PM) [9], which has been demonstrated both theoretically [10] and experimentally [11]. Utilizing such effect, a novel device is proposed in [12], which indeed works better than SJ for a lower-BV device. However, as the heavily doped N+ sidewalls are added for smaller $R_{ons}$, the PM is too weak to deplete the entire drift region fully for the long drift region device with the existence of the N+ sidewalls. As shown in Fig. 1, when the device pitch is less than 10 μm, the HK trench fully depleted the drift region and provided perfect potential distribution, which becomes merely acceptable if the device pitch is 20 μm. However, uniform potential distribution is unable to be achieved with a device pitch of 30 μm. Therefore, the device structure is unsuitable for high-voltage applications.

Literatures [9]-[12] took advantages of the PM effect from HK to achieve device performance improvement, however, the potential of the HK is yet to be brought into full play. As HK material exhibits large permittivity, it is capable of activating a strong carrier accumulation effect (CA) in silicon to significantly reduce $R_{ons}$, which has not been reported according to existing literatures. In this paper, taking advantage of both effects from HK, we propose a novel HK

trench MOS (HKTMOS), challenging the silicon limit. By the utilization of both PM and CA from HK, together with the charge balance (CB) effect, the HKTMOS achieves $R_{ons}$'s decrease by orders of magnitude and a slight BV improvement over that of SJ for both long and short drift region devices. Although such an $R_{ons}$ decrease is at the cost of a larger switching loss due to the strong CA, its figures of merit is still considerably improved compared to SJ. Moreover, HKTMOS also indicated strong BV tolerance towards the doping-imbalance between the N and P drift regions.

## II. Device Structure and Mechanism

A cross section view of HKTMOS is shown in Fig. 2(a). HKTMOS also features alternating N and P drift region pillars similar to SJ, where a layer of HK material is sandwiched in between, together with the buried oxide in the drain, the P drift region is completely isolated from the N drift region and the drain but directly contacts the gate.

Like the mechanism described in [13], although HK trench isolation exists between the N and P drift regions, mutual depletion still occurs, as the potentials in the N&P pillars could interact with each other through the HK dielectric at the device blocking state. The CB effect that guarantees uniform potential distribution for SJ also exists in HKTMOS.

In addition to the CB, the HKTMOS also exhibits PM. The total permittivity of the drift region is boosted with the introduction of the HK trench. According to [9], the slope of the electrical field in the drift region is determined by

$$\frac{\partial^2 \varphi}{\partial^2 y} = -\frac{\partial E}{\partial y} = -\frac{qN_d}{\varepsilon_0 \varepsilon_{total}} \quad (1)$$

where $N_d$ and $\varepsilon_{total}$ are the doping concentration and total relative permittivity (the permittivity relative to a vacuum, e.g., 3.85 for $SiO_2$, and "permittivity" refers to the relative permittivity in the later discussion) of the drift region, respectively. With larger $\varepsilon_{total}$, the slope of the electric field is smaller, giving better potential distribution. The mechanism of PM is explained from another angle in [7]; the fringe capacitance of the dielectric will assist in the depletion of the silicon region, and the BV is boosted even with the $SiO_2$ dielectric. For the HKTMOS with the HK trench and therefore larger fringing capacitance, the depletion assistance from the HK dielectric is much stronger than the $SiO_2$, which is enough to change the potential distribution for the power device. Furthermore, the PM effect has some similarities with [14], where a low doped drift control zone is placed in parallel with the drift zone but isolated by a dielectric. The drift control zone will have better potential distribution than that of the drift zone for its low doping concentration. Because the equipotential lines are continuous, the drift control zone therefore forces better potential distribution in the drift zone. However, as the material of the drift control zone is silicon, the improvement is limit for its low permittivity. On the other hand, the potential distribution in HK dielectric is ideally uniform, when it tries to change the potential distribution in the silicon in parallel, because of the large permittivity, it is capable of providing large amount of charges to the drift region, which is enough to give uniform potential distribution to the entire drift region.

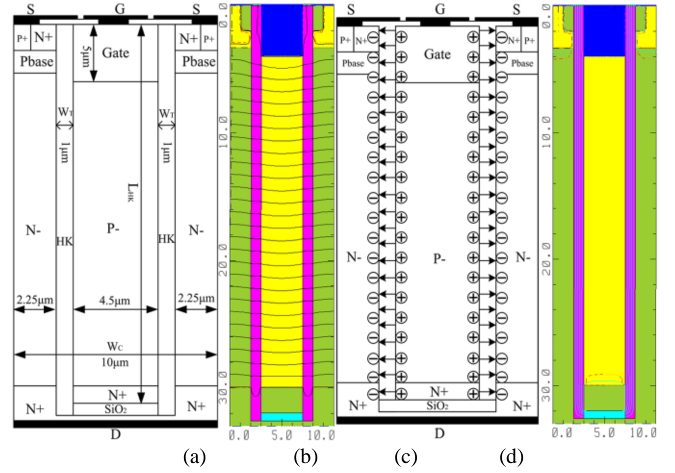



Fig. 2. (a) HKTMOS cross section view with N- and P- doping of $10^{15}$ cm$^{-3}$, Pbase doping of $3\times10^{16}$ cm$^{-3}$, P+, N+ doping of $10^{20}$ cm$^{-3}$, and channel length of 2 μm. (b) Potential distribution of HKTMOS at the block state with drain voltage of 500 V. (c) Illustration of the accumulation effect. (d) Potential distribution of HKTMOS in the on-state at the gate voltage of 15 V.

As both effects of CB and PM guarantee uniform potential distribution in the HKTMOS drift region, its BV is thereby better than the SJ that relies on CB only. As the SJ device is capable of achieving uniform potential distribution for long drift region devices, so too is the HKTMOS, whose potential distribution is almost ideal, as shown in Fig. 2(b). Apparently, there is virtually no lateral potential difference on both sides of the HK trench, and the dielectric breakdown never occurs at the device blocking state. Because both effects of PM and CB co-exist in HKTMOS, the high BV is guaranteed for not only short but also long drift region devices.

In addition to the PM, CA is another prominent feature of HK that can be utilized to improve device performance. Although the reduction of the device $R_{ons}$ by mean of CA has been reported in [15], the CA is generated through the $SiO_2$ layer, which is limited due to the low permittivity of $SiO_2$. However, the CA introduced by HK is stronger for its larger permittivity. When the device in Fig. 2(a) is in the on-state and the gate voltage is high, as the P pillar is isolated from the drain and the drift region but directly in contact with the gate, it shares the same potential as the gate. Meanwhile, both the drain and source voltages are much lower than the gate, consequently, as the potential difference exists at both sides of the trench, and the CA occurs at the interfaces of the N drift region and HK trenches, as shown in Fig. 2(c). The large permittivity of HK amplifies CA and forms high carrier density conducting paths between the drain and the source, and the device $R_{ons}$ is thereby significantly reduced. When the gate voltage is high, the HK trenches will withstand the major voltage drop, as shown in Fig. 2(d). According to [16], the minimum breakdown voltage of a potential candidate material: BZN, is 4.5V with the thickness of 100nm. Therefore, with the thickness of 1um, the BV will be 45V. Furthermore, the usage of BZN in [16] is for antifuse application, where lower BV of the dielectric is preferred and one of the targets of the BZN optimization for its fabrication condition. For the

application on the power device, we can adjust the fabrication condition for higher BV, then, much higher gate voltage is allowable. The gate voltage is below 50 V in most of applications. Therefore, the breakdown of HK dielectric will not happen in the HKTMOS.

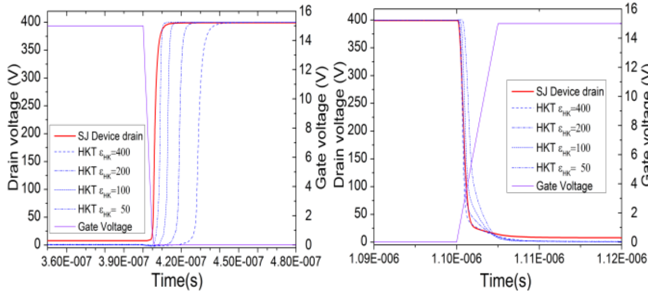



Fig. 3. The switching behavior of HKTMOS and SJ devices with device length of 39 μm under the conditions of a 15 V square wave gate voltage and 100 V drain voltage, where the drain resistance is 4×10$^6$ Ω and 4×10$^7$ Ω for HKTMOS and SJ, respectively with both dimension of 20 μm×1 μm..

CA allows significant $R_{ons}$ reduction with no extra drift region doping. However, the formation of such a low resistance conducting path requires large trench capacitance to accumulate enough charges in the on-state, which is then discharged in the off-state to guarantee high BV. The charge and discharge of that large trench capacitor cause the high loss and slow speed for the switching. The switching behaviors for SJ and HKTMOS with the parameters in Fig. 2(a) are simulated by TMA-MEDICI, as shown in Fig. 3. With a device length ($L_{HK}$ in Fig. 2(a)) of 39 μm, SJ gives the fastest switching speed; the switching delay for HKTMOS is greater than SJ and always gets worse with higher HK permittivity ($\varepsilon_{HK}$).

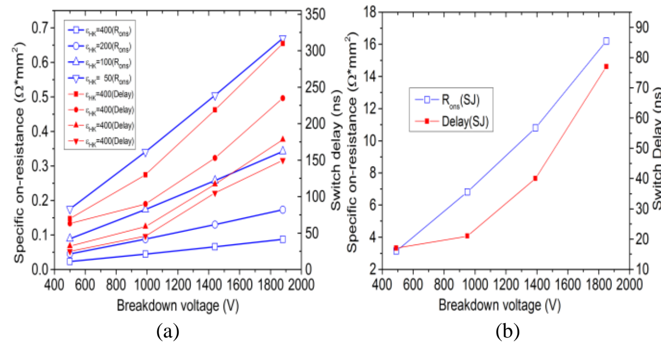



Fig. 4. Under the 15 V gate voltage, the $R_{ons}$ vs. BV and switch delay (sum of the transient rise and fall time for the drain voltage) vs. BV with a drain resistance of 4×10$^6$ Ω for HKTMOS (a) and 4×10$^7$ Ω for SJ (b) under the dimension of 20 μm×1 μm for both devices. The $R_{ons}$ and the switching delay are simulated under a drain voltage of 0.1 V and 100 V, respectively.

More detailed switching delay and $R_{ons}$ for HKTMOS and SJ are shown in Fig. 4(a) and Fig. 4(b), respectively. The $R_{ons}$ of the SJ rises rapidly at the exponential of 1.33 with the linear increase of BV [13]. In contrast, under the strong CA in HKTMOS, the $R_{ons}$ is in a linear relationship with BV and orders of magnitude lower than that of the SJ, as Fig. 4 shows. Higher $\varepsilon_{HK}$ always brings smaller $R_{ons}$, owing to the reason that larger $\varepsilon_{HK}$ provides larger trench capacitance and therefore stronger CA and smaller $R_{ons}$. In contrast, the switching delay of HKTMOS and SJ are in the totally opposite situation. The switching of SJ is fastest, as no accumulation charges exist. However, because extra time is needed to allow the accumulation charges to get into and out of the device, the HKTMOS suffers a bad switching delay, which becomes more severe with higher $\varepsilon_{HK}$.

## III. Figures of Merit Analysis

According to the previous analysis, with the introduction of the HK material, HKTMOS enjoys both BV and $R_{ons}$ improvements over SJ but at the cost of bad switching behaviors. To judge the comprehensive performance of HKTMOS, it is necessary to investigate its switching figures of merit (FOM). The FOM is defined as $R_{ons}*Q_{gd}$ [17], where $R_{ons}$ and $Q_{gd}$ are the device specific on-resistance and gate-to-drain charges, respectively. The $Q_{gd}$ for both HKTMOS and SJ are simulated as shown in Fig. 5. A 0.2 μA constant charging current is applied on the gate of the single cell for both HKTMOS and SJ, and the drain and gate voltage vs. time is as the curves in Fig. 5 indicates. The $Q_{gd}$ is defined as the integral of the gate current in the time interval from the initial drain voltage drop until the drain voltage drops to the on-state voltage, i.e., the gate voltage plateau phase [17]. Because the on-resistance of SJ is almost irrespective of the gate voltage once it has been fully turned on, the drain voltage of SJ reaches its final on-state voltage rapidly at the time of 500 ns with a constant gate charging current; the gate voltage waveform is also in good agreement with [17], in which a clear voltage plateau phase exists. However, the switch behavior of HKTMOS is totally different; as shown in Fig. 5, the drain voltage always drops and never reaches the steady state during the simulation time interval. This is because the on-resistance of HKTMOS is dependent on the gate voltage; the steady state never exists as long as the gate voltage is changing; also, there is no gate voltage plateau phase in Fig. 5b. Because the final on-state voltage of HKTMOS is related to the gate voltage, its exact $Q_{gd}$ is unable to be determined by the definition in [17].

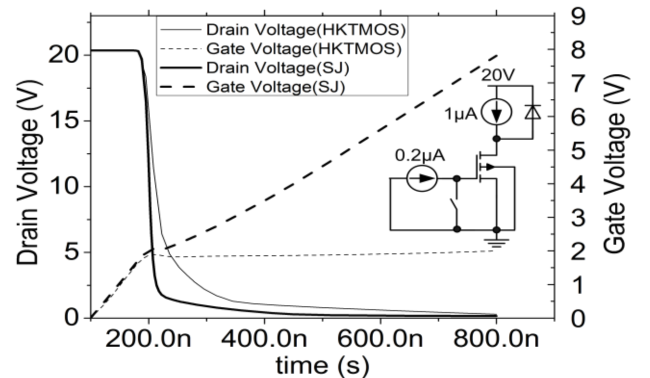



Fig. 5. The drain and gate voltage waveform with the charging of the gate by constant current for SJ and HKTMOS with the $L_{HK}$=39 μm and $\varepsilon_{HK}$=100 under the dimension of 20 μm×1 μm for both devices.

Fig. 5 also reveals the switching delay problem of HKTMOS; with the same gate charging current, the final gate voltage of SJ is much larger than that of HKTMOS (8 V vs. 1.8V, respectively) at 800 ns. The reason is that because of the large trench capacitance, HKTMOS consumes much more current during the gate charging process to allow the gate voltage to rise to the same level. Consequently, a longer

charging period is necessary, which is the major cause of its slow switching speed.

In actual applications, the gate voltage of a power device is usually higher than 10 V, and the HKTMOS needs much more gate charges than SJ to achieve the same gate voltage. Then, it is better to investigate the FOM for the product of total gate charges and $R_{ons}$ to determine the performance of HKTMOS as in [18] and [19]. The total gate charges are the integral of the gate current over the time interval when the gate voltage rises from zero to the final voltage. We define the product of $R_{ons}$ and specific total gate charges ($Q_{sg}$) as FOM(H) in this paper, after the definition of FOM(G) in [17].

For the HKTMOS device, the CA effect generates a low-resistance path between the drain and the source; together with the paralleled drift region resistance $R_{\text{drift}}$ and channel resistance $R_{\text{channel}}$, the $R_{ons}$ of HKTMOS is obtainable by:

$$R_{ons} = R_{\text{channel}} + R_A // R_{\text{drift}} . \quad (2)$$

According to [17], the accumulation resistance is $R_A \propto 1/C_g$, where $C_g$ is the unit area HK trench capacitance; $C_g$ also follows the relationship $C_g \propto \varepsilon_{HK}/W_T$, where $W_T$ is the thickness of the HK trench shown in Fig. 2(a). With large $\varepsilon_{HK}$, $R_A$ is overwhelmingly smaller than $R_{drift}$. Moreover, the $R_{channel}$ is also determined by the charges generated by HK dielectric as well as the $R_A$, which is inverse proportional to the $C_g$. Therefore, the $R_{\text{channel}}$ could be considered as a small part of $R_A$. Apparently, the device $R_{ons}$ is thereby primarily determined by $R_A$; then, we have the relationship:

$$R_{ons} = R_A \propto \frac{L_{HK}}{V_g C_g W} \propto L_{HK} \bullet \frac{W_T}{V_g \varepsilon_{HK} W} , \quad (3)$$

where $L_{HK}$, $V_g$, $W_T$, and $W$ are the device length, gate voltage, width of the cell, and width of the device perpendicular to the page, respectively.

Although the source junction and the drain not contributing to the total resistance are included in the $L_{HK}$ in (3), their length is slim to $L_{HK}$ and thereby negligible. Then, $R_{ons}$ is proportional to $L_{HK}$ from (3).

However, the total gate charges are contributed by both the HK trench capacitor ($Q_{HK}$) and the depletion charges ($Q_{DC}$) of CB. If we neglect the capacitance from bottom $SiO_2$ buries, which is overwhelming smaller than the HK trench for both permittivity and area, the specific-gate-charge $Q_{sg}$ is given by:

$$Q_{sg} = Q_{HK} + Q_{DC} . \quad (4)$$

Similar to $R_{ons}$, with large $\varepsilon_{HK}$, the $Q_{sg}$ is primarily determined by $Q_{HK}$, as it is overwhelming larger than $Q_{DC}$; then, we have:

$$Q_{sg} = Q_{HK} \propto L_{HK} \bullet V_g C_g W \propto L_{HK} \bullet V_g \varepsilon_{HK} W / W_T . \quad (5)$$

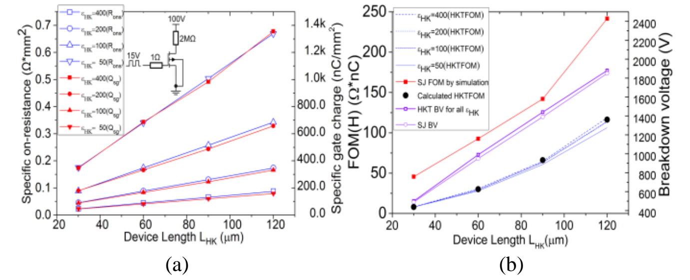
$Q_{sg}$ is proportional to $L_{HK}$ in (5). As previously discussed, $R_{ons}$*$Q_{sg}$ is the definition for FOM(H), which gives:

$$FOM(H) = R_{ons} \times Q_{sg} \propto L_{HK}{}^2 . \quad (6)$$

An interesting result is observable from (6) that for an HKTMOS with a given cell geometry, its FOM(H) is irrespective of $\varepsilon_{HK}$ and $W_T$ but only proportional to the square of $L_{HK}$. The FOM(H) for HKTMOS is therefore controllable and predictable.

## IV. Simulation Verification and Discussion

For the sake of the objective FOM(H) comparison between SJ and HKTMOS, the target devices under the condition of same dimension and similar BV are necessary. As the co-existence of PM and CB effect, the BV of HKTMOS is higher than that of the SJ and shows strong tolerance towards the varying of the drift region doping. Whereas the BV of the SJ is sensitive to the drift region doping [20]. Consequently, the drift region doping of SJ must be low to achieve similar BV with HKTMOS and therefore an objectively FOM(H) comparison. The drift region doping concentration is chosen to be $10^{15}$cm$^{-3}$ for both SJ and HKTMOS in our subsequent simulation and discussion.




(a) (b)

Fig. 6. The $R_{ons}$ (simulated under 15 V gate voltage and 0.1 V drain voltage) and $Q_{sg}$ (simulated by the integral of the gate current as the schematics show in the figure) vs. $L_{HK}$ for HKTMOS (a) The FOM(H) vs. $L_{HK}$ for HKTMOS by both simulation and calculation, together with the FOM(H) of SJ and BV by simulation (b).

The simulated values for $R_{ons}$ and $Q_{sg}$, with size and doping in Fig. 2(a) but varying $L_{HK}$, are shown in Fig. 6(a). $R_{ons}$ is simulated under the condition of a 15 V gate voltage and 0.1 V drain voltage. $Q_{sg}$ is simulated schematically as shown in Fig. 6(a), where a 15 V square wave voltage is applied on the gate. $Q_{sg}$ is determined by the current integral at the time interval when the drain drops from 100 V to the voltage of the fully on-state. As Fig. 6(a) shows, both $R_{ons}$ and $Q_{sg}$ increase linearly with the rise of $L_{HK}$, which is consistent with (3) and (5). (3) and (5) also indicated that $R_{ons}$ and $Q_{sg}$ are proportional and inversely proportional to $\varepsilon_{HK}$, respectively. The relation is also verified by simulation, as Fig. 6a shows; a larger $\varepsilon_{HK}$ always provides a smaller $R_{ons}$ but a larger $Q_{sg}$ and vice versa.

Fig. 6(b) shows the FOM(H) and BV vs. $L_{HK}$ for both HKTMOS and SJ, where the FOM(H) of HKTMOS with changing $\varepsilon_{HK}$ are plotted in different line styles. As mentioned above, $R_{ons}$ and $Q_{sg}$ are inversely proportional and proportional to $L_{HK}$, respectively, which cancel each other out when the multiplication for FOM(H) occurs. It can be observed that all of the lines almost overlap with each other for different $\varepsilon_{HK}$ when $L_{HK}$ ranges from 30 μm to 120 μm (Fig. 6(b)) according to simulation, which agrees with (6) very well. The proportional coefficient between the FOM(H) and $L_{HK}$ square may be different depending on the cell geometry;

however, for a device with a given cell geometry, the FOM(H) is only determined by $L_{HK}$ regardless of the HK permittivity and trench thickness.

For HKTMOS with the size displayed in Fig. 2(a), the analytical value of the proportional coefficient is derived as $7.812\times10^{-3}$ $\Omega$*nC/μm$^2$. Utilizing such a coefficient, we are able to calculate the FOM(H) using (6), which is shown by the round dots in Fig. 6(b). It is clear that the calculation results agree well with the simulation results. Fig. 6(b) also reveals that for the HKTMOS with smaller $\varepsilon_{HK}$ ($\varepsilon_{HK}$=50), the FOM(H) by simulation is slightly smaller than the calculated value, especially at larger $L_{HK}$. This is because $Q_{sg}$ is determined by the sum of $Q_{HK}$ and $Q_{DC}$, then, $Q_{sg}$ will drop linearly with the linear decrease of $\varepsilon_{HK}$ as long as $Q_{HK}$ is still larger than $Q_{DC}$ according to (4). However, as $R_A$ parallels with $R_{drift}$, with smaller $\varepsilon_{HK}$, $R_A$ in (2) is less dominant, and the contribution to $R_{ons}$ from the drift region $R_{\text{drift}}$ becomes more significant although $R_A$ is still much lower than $R_{\text{drift}}$. Consequently, the total $R_{ons}$ will rise sub-linearly with the decrease of the small $\varepsilon_{HK}$ due to the contribution from the drift region bypass, which has been neglected in previous analysis. Moreover, according to (6), the FOM(H) of HKTMOS is proportional to the square of $L_{HK}$; the square amplifies the model inaccuracy if $L_{HK}$ is large, which causes a larger FOM(H) difference between the calculated and simulated values under the condition of a large $L_{HK}$ and a small $\varepsilon_{HK}$ as shown in Fig. 6(b).

Fig. 6(b) also shows the relationship between BV and $L_{HK}$ for both HKTMOS and SJ. The BVs of HKTMOS with different $\varepsilon_{HK}$ completely overlapped with each other so that only one curve is shown for HKTMOS. As the BV of SJ relies on CB only, while HKTMOS takes both effects of PM and CB to achieve high BV, the BV of HKTMOS will be slightly better than that of SJ, as shown in Fig. 6(b). Last but not least, HKTMOS always demonstrates significant FOM(H) improvement over that of SJ under all $L_{HK}$ in the figure; the FOM(H) of HKTMOS is 48% of that of SJ at the $L_{HK}$ of 120 μm, and only 17% at the $L_{HK}$ of 30 μm. Although the FOM(H) takes the total gate charges into consideration instead of the gate-to-drain charges only, HKTMOS still exhibits a significant FOM(H) improvement over that of SJ.

Further investigations are made for HKTMOS with changing parameters. Fig. 7(a) shows the $R_{ons}$ and $Q_{sg}$ for an HKTMOS under varying cell size $W_C$ but fixed $W_T$ and $L_{HK}$, which are 1 μm and 39 μm, respectively. As a larger $W_C$ suggests less HK trench proportion in the device, there are fewer accumulation conduction channels for a device with a given area, and $R_{ons}$ is therefore increased; also, with a lower HK proportion, fewer accumulation charges are needed; therefore, $Q_{sg}$ decreases with the increase of $W_C$ and vice versa. The increase of $R_{ons}$ and the decrease of $Q_{sg}$ are both linear, providing a constant product: the FOM(H) as shown in Fig. 7(b). The FOM(H) for HKTMOS remains unchanged for a $W_C$ ranging from 8 to 12 μm, and the curves also overlap for FOM(H) under different $\varepsilon_{HK}$. $L_{HK}$ is the only parameter that changes the FOM(H) for HKTMOS. The simulation results also agree with (6) well. Fig. 7(b) also shows the FOM(H) for SJ under the same size condition as HKTMOS; because of the JFET effect, its FOM(H) rises with the shrinking of $W_C$, especially when $L_{HK}$=120 μm and $W_C$=8 μm; the FOM(H) of SJ experiences a sharp rise at that point because of the JFET effect becoming dominant, which causes a large $R_{ons}$. In contrast, HKTMOS is free of the JFET effect, and its FOM(H) therefore remains unchanged for different $W_C$. Apparently, the FOM(H)s of HKTMOS are always better than the same sized SJ (Fig. 7(b)).

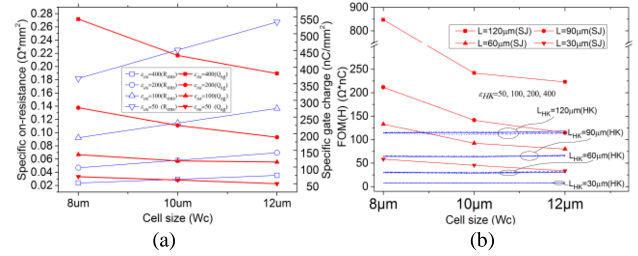



Fig. 7. The impact of cell size $W_C$ to $R_{ons}$ and $Q_{sg}$ for an HKTMOS with $L_{HK}$=39 μm (a). The FOM(H) vs. $W_C$ for SJ and HKTMOS with different $\varepsilon_{HK}$ and device length (b), where L and $L_{HK}$ are the device length.

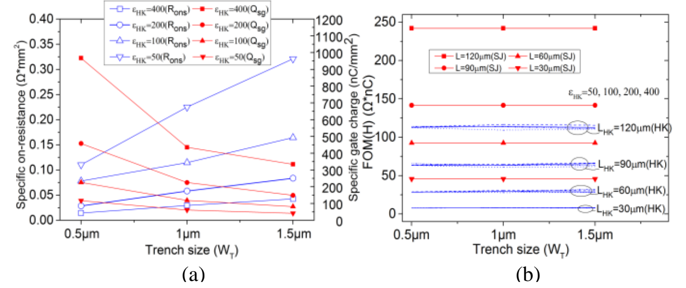



Fig. 8. The impact of trench width $W_T$ to $R_{ons}$ and $Q_{sg}$ for an HKTMOS with $L_{HK}$=39 μm (a). The FOM(H) vs. $W_T$ for SJ and HKTMOS with different $\varepsilon_{HK}$ and device length (b), where L and $L_{HK}$ are the device length.

The impact of trench width ($W_T$) on device performance is shown in Fig. 8. A thinner trench always causes a stronger accumulation effect, which causes a smaller $R_{ons}$ and larger $Q_{sg}$ and vice versa. As shown in Fig. 8(a) for an HKTMOS with an $L_{HK}$ of 39 μm, $R_{ons}$ and $Q_{sg}$ are proportional and inversely proportional to $W_T$, respectively, which agrees with (3) and (5) well. Therefore, the product of $R_{ons}$ and $Q_{sg}$, i.e., the FOM(H) with given $L_{HK}$, is a constant, as Fig. 8(b) reveals. The FOM(H) for SJ with the same size as that of HKTMOS is also shown in Fig. 8(b). Because no trenches exist for SJ, the FOM(H) for SJ in Fig. 8(b) is a constant for the change of the trench width parameter of HKTMOS; however, it is still larger than HKTMOS under the same size condition.

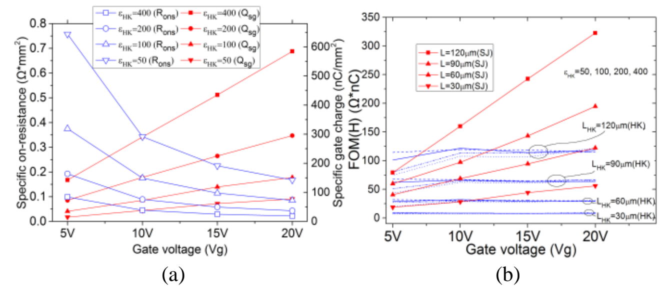



Fig. 9. The impact of the gate voltage $V_g$ to $R_{ons}$ and $Q_{sg}$ for an HKTMOS with $L_{HK}$=39 μm (a). The FOM(H) vs. $V_g$ for SJ and HKTMOS with different $\varepsilon_{HK}$ and device length (b), where $L$ and $L_{HK}$ are the device length.

Fig. 9a reveals the changes of $R_{ons}$ and $Q_{sg}$ as the gate voltage ($V_g$) ranges from 5 V to 20 V for an HKTMOS with an

$L_{HK}$ of 39 μm. The higher $V_g$ definitely accumulates more charges, which suggests smaller $R_{ons}$ but larger $Q_{sg}$. According to (3) and (5), $Q_{sg}$ and $R_{ons}$ are proportional and inversely proportional, respectively to $V_g$, a result that is consistent with the simulation results in Fig. 9(a). The FOM(H)s for both HKTMOS and SJ are shown in Fig. 9b. However, the FOM(H) curves of HKTMOS for different $\varepsilon_{HK}$ did not overlap completely as in Fig. 7(b) and Fig. 8(b), especially under the condition of smaller $\varepsilon_{HK}$ and lower $V_g$. The reason is similar to that behind the difference between the calculated and simulated values of the FOM(H) in Fig. 6(b). With lower $V_g$, the accumulation effect is weakened; the contribution of $R_{ons}$ from $R_A$ becomes less dominant as $R_{\text{drift}}$ is more significant. As a result, the relationship between $R_{ons}$ and $\varepsilon_{HK}$ becomes sub-linear under the conditions of a smaller $\varepsilon_{HK}$ and a lower $V_g$, whereas $Q_{sg}$ still maintains a linear relationship with $\varepsilon_{HK}$. As shown in Fig. 9(b), the FOM(H)s of HKTMOS no longer remain constant with the changing of $\varepsilon_{HK}$ at a small $V_g$. The FOM(H)s of HKTMOS with different $\varepsilon_{HK}$ overlap at higher gate voltage because $R_A$ dominates $R_{ons}$ again. The FOM(H)s of SJ with the same size under different gate voltages are also plotted in Fig. 9(b). As no CA exists, the $R_{ons}$ of SJ is irrespective of the gate voltage; however, the $Q_{sg}$ for SJ will always rise with the gate voltage, and consequently, the product of $R_{ons}$ and $Q_{sg}$ for SJ will rise linearly with the gate voltage.

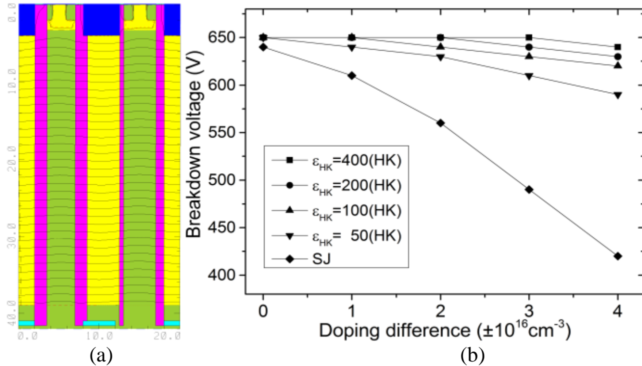



Fig. 10. (a) The potential distribution for a HKTMOS with $L_{HK}$ of 39 μm and HK trench randomly shifted in both width and position. (b) The impact of charge-imbalance to BV for SJ and HKTMOS with different $\varepsilon_{HK}$ for the device length of 39 μm under the baseline doping of $10^{15}$ cm$^{-3}$ for both N and P pillar.

The charge-imbalance between the N&P drift region in the fabrication process is another issue of SJ; even a slight charge-imbalance caused by doping differences can severely impact BV. Adversely, HKTMOS exhibits excellent doping difference tolerance because its BV not only depends on CB but also PM. Because the CB and PM are the separated effects, the fluctuation of position and width of the trench have no impact to the charge balance and the potential distribution in HKTMOS still remains uniform with as Fig. 10(a) shows. Furthermore, as shown in Fig. 10(b), with the rise of the N&P drift region doping difference, the BV of HKTMOS with $\varepsilon_{HK}$=400 remains almost unchanged. However, a smaller $\varepsilon_{HK}$ value causes higher BV sensitivity to the doping difference. This is because a smaller $\varepsilon_{HK}$ value always impairs the PM capability of the HK trench, and the BV therefore drops more rapidly with the rise of the doping difference. As the BV of SJ relies only on the CB and is free of PM, SJ gives the worst tolerance, as shown in Fig. 10. The BV of SJ at a doping difference of $4\pm10^{16}$cm$^{-3}$ drops to 60% of the BV under the charge-imbalance condition.

Although the HKTMOS realizes $R_{ons}$ reduction at the cost of the larger switching loss, it is possible to transfer the significant decrease of the $R_{ons}$ of the HKTMOS to the area instead of $R_{on}$. With smaller area and less number of the cells, the trench capacitance will be smaller, and switching loss is significantly reduced. As shown in Table I, with BV and $R_{on}$ of 650V and 29.5mΩ, respectively, the width of SJ will be much larger than that of the HKTMOS for its high $R_{ons}$. However, the switching loss of the HKTMOS is only half of the SJ. As the switching loss and the $R_{ons}$ of HKTMOS are proportional and inverse proportional to the $\varepsilon_{HK}$, respectively, the switching loss of the HKTMOS is almost irrespective of the HK permittivity. As a result, although the $R_{on}$ of the SJ and HKTMOS are same, the area down is gained with even smaller switching loss for HKTMOS. In another word, the HKTMOS could bring the same or better performance than that of the SJ under the condition of much smaller device size, which is attractive for the commercial application.

TABLE I: THE SWITCHING LOSS ENERGY FOR SJ AND HKTMOS WITH BV AND RON OF 650 V AND 29.5 MILLIOHMS

| DEVICE TYPE | DEVICE WIDTH | SWITCHING LOSS |
|---|---|---|
| SJ | 87.89μm | 243.53 pJ |
| HKTMOS($\varepsilon_{HK}$ =400) | 1μm | 120.04 pJ |
| HKTMOS($\varepsilon_{HK}$ =200) | 1.97μm | 120.30 pJ |
| HKTMOS($\varepsilon_{HK}$ =100) | 3.88μm | 116.58 pJ |
| HKTMOS($\varepsilon_{HK}$ =50) | 7.62μm | 114.24 pJ |

## V. FABRICATION AND MATERIAL CONSIDERATION

The fabrication of HKTMOS is difficult but not impossible. The prospective fabrication process is as shown in Fig. 11(a), the first step is partial oxide ion implantation to form the $SiO_2$ burier layers. As discussed in [21] and [22], the $SiO_2$ burier isolations could be formed inside of the silicon substrate by high-energy oxide ion implantation with a hard mask. Because the $SiO_2$ burier layer is internal to the substrate instead of on the surface, the P- or N- can be epitaxial grown on the substrate and then doped to form the alternating structure as shown in Fig. 11(b). In succession, the trench is etched by RIE, as shown in Fig. 11(c), which is followed by the trench filling of HK material in Fig. 11(d). Next, for a low BV device with a short device length, where the trench depth-to-width ratio is within the limit of the HK material trench filling process, the next step jumps ahead to that in Fig. 11(g). After the removal of the HK material on the surface, the silicon is epitaxially grown and doped again to form the P-base, P+ trench gate, N+ source, and P+ ohm contact. For a high BV device with a long drift region, the HK is unable to be fully filled at such a depth trench in one step; then, the multiple epitaxial growth and trench filling process is undertaken. As shown in Fig. 11(e) and Fig. 11(f), after the trench filling in Fig. 11(d), the HK on the surface is removed and the P- or N- is epitaxially grown and doped again; then, the trench is etched by RIE and filled with HK, as shown in

Fig. 11(f). The process from Fig. 11(e) to Fig. 11(f) is repeatable multiple times until the desired drift region length is achieved. After that, the P-base, P+ trench gate, N+ source, and P+ ohm contact are formed, as shown in Fig. 11(g), and finally, the HK material is filled in the trench to form the gate dielectric and etched to make the metal contact for the gate and source in Fig. 12(h).

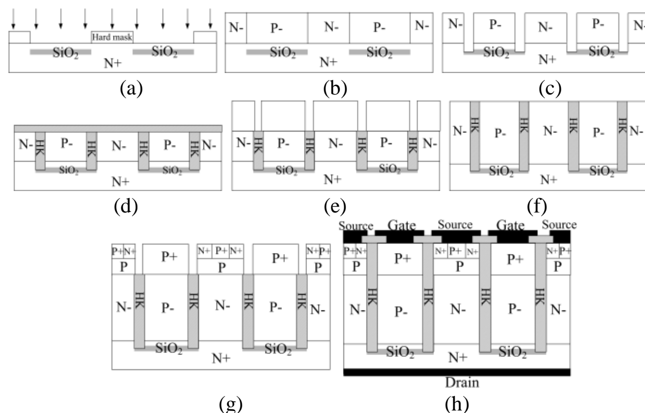



Fig. 11. The major fabrication process steps of HKTMOS.

The candidate HK materials for HKTMOS include PZT, BST, STO, BZN, etc. All of the above materials could realize permittivity at several hundreds scale [23]-[25]. The pre-annealed permittivity for PZT is approximately 200 according to our experimental result [11]. The post-annealing permittivity of the strontium-modified PZT even reaches the thousands scale [26], which is absolutely enough for HKTMOS. PZT could be filled inside of the trench by the Sol-Gel method and is capable of withstanding high temperatures for the silicon process, which is a possible solution for HKTMOS fabrication. Another solution is the pseudo-HK material proposed in [27]; the mixture of metal particles and polyimide will demonstrate HK behaviors, which has been experimentally verified in [28]. The pseudo-HK material can be deposited by CVD, which is easier for the filling of the trench with a larger depth-to-width ratio. The permittivity of pseudo-HK material is determined by the quantity of metal particles in polyimide [28]; the permittivity at several hundreds scale is also realizable.

## VI. Conclusion

The HKTMOS we proposed in this paper exhibits excellent performance for a wide BV range according to investigation. Its FOM(H) is predictable and shows significant improvement over that of SJ. Moreover, HKTMOS also demonstrates its good charge-imbalance tolerance in comparison to its SJ counterparts. Above all, HKTMOS has potential for application in energy conversion systems for better efficiency and further promotion of the silicon limit.

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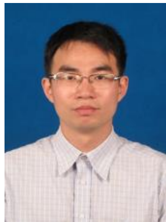

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