Asynchronous 10MS/s 10-Bit SAR ADC for Wireless Network

Yulin Zhang, Guiliang Guo, Yuepeng Yan, and Tao Yang

***Abstract*—This paper presents a low power asynchronous 10-bit Successive Approximation Register (SAR) ADC implemented in 0.18μm CMOS process. The ADC is realized fully differentially with a split capacitor array to lower power cost and improve the speed. To further enhance power efficiency and high speed for a relatively moderate resolution, a new asynchronous dynamic logic is utilized to lower the digital power. The multiple-phase clock is generated by a ring-oscillator structure which avoids the high external clock. Offset of the dynamic clocked-comparator is also calibrated through adjusting the threshold voltage. The ADC consumes 500uw at Vdd=1.8v and 10M/s sampling rate.**

***Index Terms*—SAR analog to digital converter (ADC), low power, fully dynamic comparator, CMOS, offset cancellation, asynchronous logic.**

I. Introduction

As advanced CMOS technologies enhance the operational speed of logic circuit significantly. Successive approximation register (SAR) analog-to-digital converter is compatible with the standard CMOS process with low supply voltage, because it does not need operational amplifiers. The only analog part is the comparator, whose design is close to that of a digital regenerative latch. Therefore SAR analog-to-digital converters find a sweet spot in the space around 8-12b resolution and several MS/s sample rare which used to be dominated by pipelined ADCs [1]. There have been many related works to enhance the performance of the SAR ADCS. These works mainly focus on charge recycling [2], timing control [3] and comparator structure [4]. This work proposes a multiple-phase clock generation based on ring-oscillator structure with dynamic logic to optimize both the speed and power. Vcm-based switching method [2] and split capacitor array are also adopted to improve power efficiency. For better common-mode noise rejection and less distortion, a fully differential circuit structure is applied. Moreover, this paper utilizes a fully dynamic comparator with offset calibration.

The rest of this paper is organized as follows. Section II illustrates the architecture of the proposed SAR ADC. Section III describes the circuit implementation and the digital algorithm in detail. The simulation results and the conclusions are provided in Sections IV and V, respectively.

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II. SAR ADC Architecture

The block diagram of the proposed SAR ADC is described in Fig. 1. The main components of the SAR ADC are a 10bit split-capacitor DAC with bootstrapped switches, a two stage dynamic comparator with an offset calibration, internal clock generation, and an asynchronous SAR controller. The SAR ADC samples the input signal when the CLK=1. During CLK=0 (conversion phase), the ADC completes ten comparisons for 10-b conversion based on an internal clock CKC, which is produced by a ring oscillator loop consisting of the dynamic comparator and delay elements. Section III describes internal clock generation in detail.

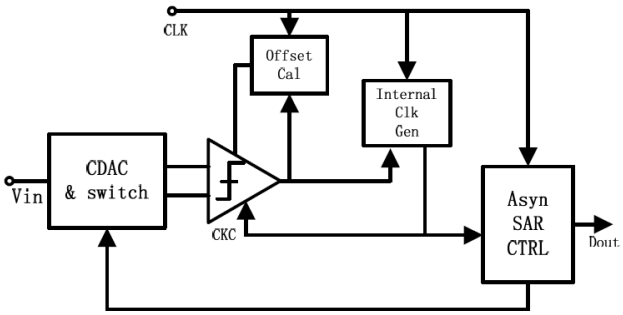

Fig. 1. SAR ADC architecture.

III. Circuit Implementation

A. DAC Network

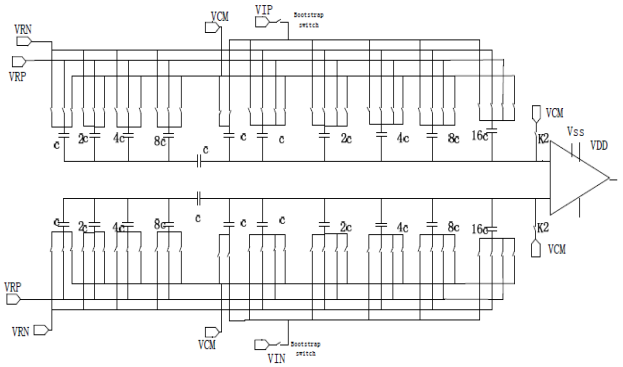

Fig. 2. Split DAC capacitor array.

Switching the capacitor array consumes significant power. The value of unit capacitance needs to be minimized which is limited by mismatch and KT/C noise. Therefore the split capacitor array [5] is adopted to save power. By utilizing effective switching approaches, further power saving is obtained. The set-and-down method [6] saves significant energy. However during the conversion process, the common

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mode of the reference voltage gradually decreases from half reference voltage to ground. Fig. 2 shows the DAC (digital to analog converter) structure. The Vcm-based switching is adopted which is more power efficient and also obtains half-capacitance reduction. The DAC structure is a split binary capacitor array designed with the upper 5 bit MSB and lower 4 bit LSB arrays. The bridge capacitor of a split capacitor array in the conventional architecture is fractional value that is difficult for layout. In this DAC structure, the bridge capacitor is a unit capacitor.

During sampling phase, all the capacitors in MSB array and a dummy capacitor are charged to the analog signal; meanwhile the comparator and capacitors in LSB array are attached to Vcm (common mode voltage). Then By switching all of the MSB capacitors to Vcm, the conversion starts. In this phase, the DAC output finally settles to [7]:

$$V_0 = K\left(V_{in} - \frac{V_R}{C_{IN}}\left(\sum_{i=1}^{N} b_i \times 2^i \times C_u\right)\right) \quad (1)$$

where,

$$K = \frac{C_{IN}}{C_{total}} \quad (2)$$

The C_{IN} is the total capacitance attached to V_{IN} (input signal) during the sampling phase, the C_{total} is the total capacitance at the output node, and the digital codes bi are determined by binary searching arithmetic to control the capacitor switches. V_R is the differential reference voltage and C_u is the unit capacitor. The coefficient K has no effect on the linearity of the analog to digital conversion.

In this design, the unit element capacitor of the DAC converters is set to 42 fF to reduce nonlinearity caused by mismatch. The total amount of input load capacitance is 32 C. This means that the input load capacitance is 1.35pF, which is large enough to meet the noise requirement for covering process variations. The switches in the CDAC are connected to VRP, VRN or VCM. They are designed by using either NMOS or PMOS to save the area and power. In order to suppress distortion during analog signal sampling, Bootstrapped switches based on [8] are employed.

B. Dynamic Comparator with Offset Cancellation

As is shown in Fig. 3, the comparator is a two stage dynamic comparator [4] which is quite power efficient. The first stage is a voltage ampliation stage with a differential pair. The latching stage contains a positive-feedback amplifier to obtain the rail to rail digital output. Before the comparison, the ampliation stage output is charged to near VDD. A rising CLK edge stops the pre-charging and starts the ampliation in the first stage. Then the common voltage of the output of the first stage decreases when it approaches the threshold of the input of the second stage, the feedback back-to-back inverters was triggered to provide the output. This comparator has no power dissipation when the comparator is not active.

As this type of dynamic comparators cannot apply analog feedback, and auto-zeroing is also discarded. For the dynamic comparator, the offset voltage can be canceled through adjusting the load capacitance [9], the current [10], [11] or the threshold voltage of the differential pair. However, the method of controlling the load capacitance degrades the response. The current calibration technique introduced in [10] exploits additional one pair of NMOS compensation transistors in parallel with the differential input pair and a charge pump. But the calibration process has to be done frequently since the charged voltage in the compensation capacitor falls down due to the leakage current. In addition, the calibration speed and accuracy are limited by the size of the charging or discharging current sources of charge pump. Therefore adjusting the differential pair's threshold voltage technique is chosen.

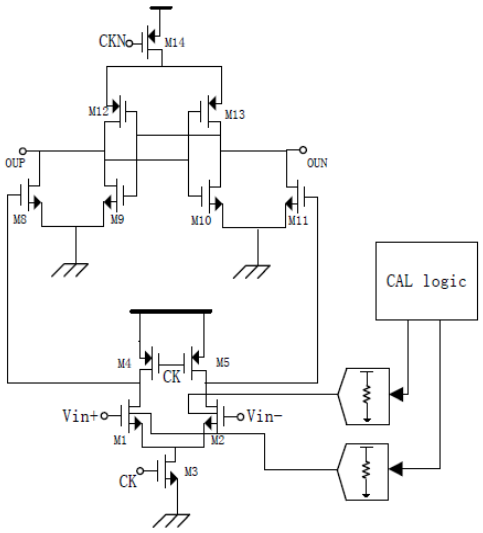

Fig. 3. Circuit schematic of the offset calibration scheme.

Fig. 4 shows the architecture, M1 and M2 are deep well NMOS transistors for good noise performance. And their substrate voltages can be forwarded to change the threshold voltages of the differential pairs. Thus the difference between the current of the input pair is minimized. The offset cancellation is realized by connecting the differential analog input of the comparator to the common level. And the substrate terminals of the input pair are initially connected to ground (0 V). Several comparisons are made to avoid thermal noise effects inherent in the comparator. The final result is determined by the majority value and is stored in the register [12]. If the result is the same as the previous one, either or is raised accordingly to reduce the offset voltage. This routine is continued until the result reverses. The comparator offset cancellation then finishes by fixing the voltage of the substrate terminals. The body biasing is controlled by a resister DAC. The resistor DAC dissipates 15uA. In this design, a 6bit resister DAC is applied to tune the body biasing [13]. The offset distribution with an error smaller than 0.25 LSB should be covered by carefully designing the unit step and dynamic range. And this technique does not have a response penalty and does not require sensitive timing control.

C. Proposed Asynchronous SAR Logic

The sequential operation of the SA algorithm has traditionally been a limitation on the high-speed applications, because a synchronous approach relies on a clock to divide the conversion phase into equally timed slots as the conversion proceeds from MSB to LSB [14]. This internal clock for N bit ADC would therefore operate at a frequency of at least the N × sampling clock, and if only the switching power is

considered, would require at least N × the clock power of an asynchronous approach in which the sampling frequency sets the highest clock rate [15]. Asynchronous processing is more power efficient for avoiding the need for such a clock. If it were synchronous, the percentage of the total power for the clocks would rise from15%, to above 50% [16]. The logic of the SAR ADC performs a binary search algorithm. This paper proposed a ring oscillator structure to generate the multiple-phase clock. As shown in Fig. 4, the asynchronous SAR logic consists of three parts: the oscillator ring loop, the sequencer and the DAC control. The oscillator loop generate the internal high frequency clock, then the NAND gates and DFF combined to produce the bit chosen signal witch decide the DAC switch control signals and store the output data through the registers. This sophisticated SAR control logic makes single bit conversion simple without extra delay, which minimizes the delay time between the comparator regenerated output and the DAC control signals, thus a higher sample rate can be achieved. Inverters are added after the comparator to enhance the load ability and separate the noise from the digital logic. In this ring loop, the delay element is to adjust the set-up time of the DAC.

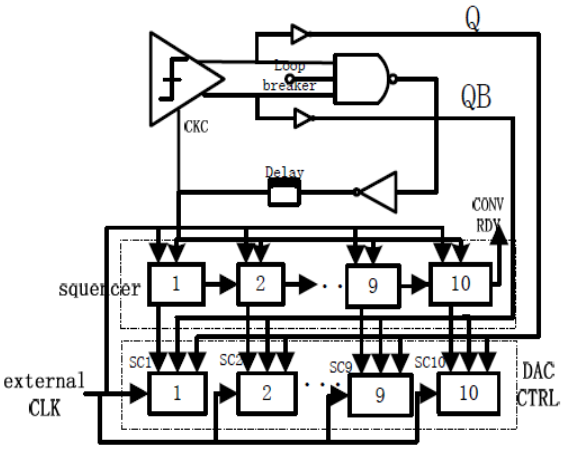

Fig. 4. Circuit schematic of the asynchronous SAR logic.

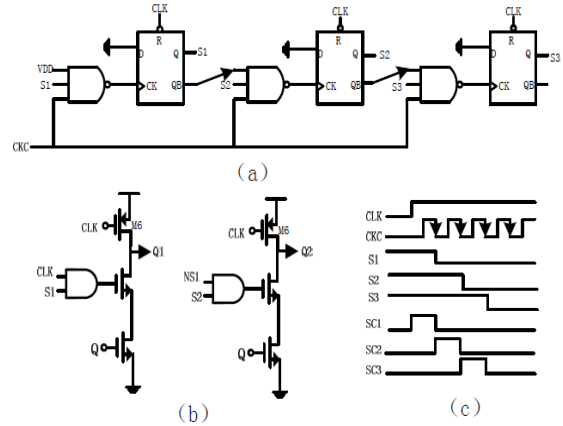

Fig. 5(a). Sequence control circuit (b). dynamic DFF to store digital output (c). timing program of Asynchronous SAR control.

In Fig. 5 (a), NAND gates and DFF are utilized to produce the sequence shifter. NAND gates are applied to guarantee the DFF only receive one clock pulse to reduce high frequency node to the DFF for lower power. In Fig. 5 (c), the asynchronous CKC is generated by the ring oscillator triggered by external CLK. The sequential signal S1, S2 cooperate the CLK to produce the SC1, SC2 witch are applied for controlling the switch logic and bit registers to store the corresponding bit comparison results. In addition, dynamic logic is applied to enhance the asynchronous processing speed and save power.

IV. Experimental Results

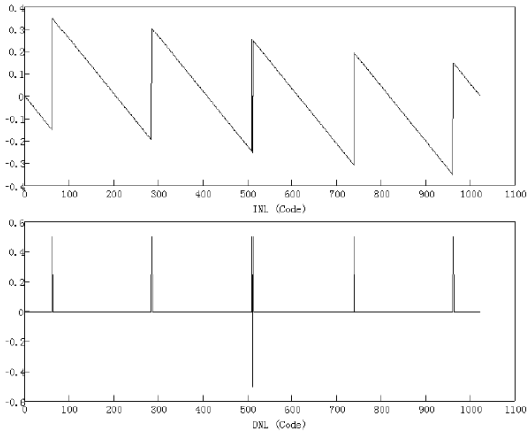

Fig. 6. Behavioral simulation of DNL and INL.

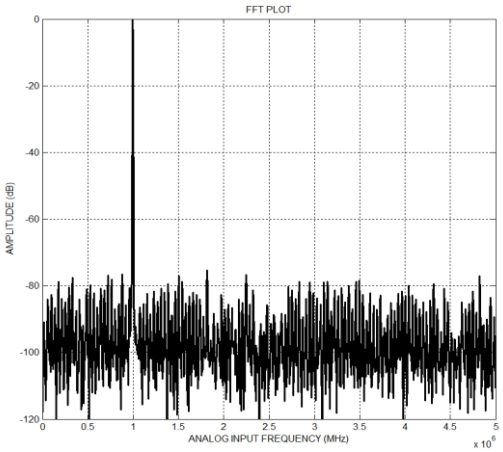

Fig. 7. FFT spectrum of 10-bit SAR ADC @Fin=996.09KHz.

TABLE I: The Performance of the ADC

process	0.18um CMOS
Sampling Rate	10MS/s
Supply Voltage	1.8v
resolution	10bit
ADC power	500uW
Input range	Rail-to-rail
DNL	+0.503/-0.5
INL	+0.35/-0.38
SNDR	61.1691dB
SFDR	79.06dB
ENOB	9.87
FOM	55fJ/step

The 10bit SAR ADC is based on 0.18μm 1.8V CMOS process, the ADC is simulated in transistor-level by Spectre at 1.8 V supply and 10MS/s.

Fig. 6 shows the static performance of the ADC. The DNL and INL are 0.503/-0.5 and 0.35/-0.38 LSB respectively. Fig. 7 shows the the simulated FFT of 1024 output spectrum when ADC operating at 10M sampling rate with an input of 1M Hz.

Table I summarizes the simulated performance of the 10-bit

10MS/s SAR ADC.

V. Conclusion

In this paper, a low power asynchronous 10bit SAR ADC was proposed for wireless network. The ring oscillator structure asynchronous dynamic logic leads to lower power and higher speed. A dynamic comparator with offset cancellation and Vcm-based switching method is adopted to further enhance power efficiency. The simulation shows that, at 1.8V supply and 10MS/s sampling rate, the ADC achieves an ENOB of 9.87 bits and consumes 500μW.

Acknowledgment

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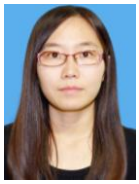

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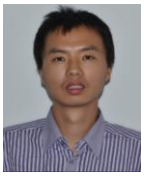

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