On the Design of a Reconfigurable Radio Processor Using FPGA

Amiya Karmakar, Amrita Saha, and Amitabha Sinha

***Abstract*—High performance DSP processors are unable to meet the speed requirements of Software Defined Radio (SDR), System on chips (SOCs) are also not suitable because of their limited flexibility. Recently dynamically reconfigurable FPGAs have emerged as high performance programmable hardware to execute highly parallel, computationally intensive signal processing functions efficiently. Since basic intention of SDR is to implement different modulation or demodulation schemes and basic building blocks for these schemes are signal processing functions, FPGAs have become an important platform for implementing SDR. Keeping these issues in view, this paper proposes a flexible architecture that combines five different modulation schemes. FPGA based implementation of the proposed architecture reveals that the number of LUTs is reduced by 11.11% compared to the sum of individual LUTs used for each of the modulation scheme. Not only LUTs but also other FPGA components like slices, bounded IOB, BESL etc. are also reduced.**

***Index Terms*—Application specific integrated circuits (ASIC), configurable logic block (CLB), common block diagram elimination method (CBDEM), communication schemes, digital signal processor (DSP), field programming gate array (FPGA), hardware description language (HDL), look up table (LUT), software defined radio(SDR), silicon utilization factor.**

I. Introduction

In conventional radio systems, parameters defining the modulation/demodulation methods, waveforms, signal generation and link layer protocols are based on fixed hardware where a set of hardware elements perform signal processing functions. The SDR [1]-[6] technology aims to overcome these limitations by offering flexible radio systems that can be upgraded efficiently by providing software control of a variety of modulation / demodulation techniques. Thus, this technology offers potentially longer product life and the radio can be upgraded efficiently, where efficiency can be measured by the cost and the physical volume consumed per information bit.

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A. Karmakar is with the West Bengal University of Technology in the Department of Computer Science of Engineering, BF-142, Sector 1, Salt Lake City (e-mail: amiya.karmakar@gmail.com).

A. Saha is with the Department of Electronics & Communication Engineering, Neotia Institute of Technology Management & Science Institution affiliated to West Bengal University of Technology and AICTE approved Degree College. Campus: Sarisa, Diamond Harbour Road, South 24 parganas, West Bengal (e-mail: inchargetandp@nitmas.edu.in).

A. Sinha is with Neotia Institute of Technology Management & Science Institution affiliated to West Bengal University of Technology and AICTE approved Degree College as a Principal. Campus: Sarisa, Diamond Harbour Road, South 24 parganas, West Bengal (e-mail: amitabha.sihna@wbut.edu.in or principal@nitmas.edu.in).

Since signal processing functions for the communication systems in SDR are represented in software, so modern SDR is implemented by simply downloading a new program in the desired system.

Utilizing parallelism in the context of sequential Von-Neumann or Harvard Architecture oriented processors has become increasingly inefficient. The advantage of executing computationally intensive functions at hardware speed resulted in the emergence of "Application Specific Integrated Circuits (ASIC)". Even though ASICs offer highest possible performance at lowest silicon cost, they suffer from inflexibility. Conventional DSP Processors [7], [8] have a set of arithmetic and control instructions optimized for signal processing algorithms and even though efficient instruction level pipelining is achieved by incorporating Harvard Architecture, and limited parallelism is achieved by VLIW architecture, performance is below the level required for many high end applications.

Field Programmable Gate Arrays (FPGA) [9]-[11] are high performance programmable hardware and have emerged with an additional feature "dynamically re-configurable" which makes them attractive in many signal processing applications. Since FPGAs are flexible programmable hardware, any architecture can be easily be scaled. Keeping these issues in view, this paper presents a novel scalable and flexible architecture and explores the possibility of implementing such an architecture using FPGAs.

II. General Overview of the Architecture of an SDR

SDR can be defined as a radio communication system that uses software to modulate or demodulate radio signals. Hence by changing the software, any given communication scheme can be implemented even in the run time. Therefore, the systems can achieve high flexibility at a lower cost than traditional analogue systems.

The implementation of a software defined radio is based on two popular concepts. The first approach is to programme a conventional DSP processor which is based on Harvard architecture, an extension of Von-Neumann architecture. So, by changing the program a desired modulation scheme can be established. Second approach is to configure a Programmable hardware by using "Hardware Description Language (HDL)" [12], [13]. Thus by changing the program, the hardware device can be configured to a particular modulation scheme. By taking the advantage of the programmable hardware like FPGA, it is possible to overcome the limitation of the conventional DSP Processors where most of the instructions are executed sequentially.

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III. FPGA Based Implementation of SDR

A. Overview of FPGAs

Configurable Logic block (CLB) which is based on the concept of "Look Up Table (LUT)" based, Routers or Interconnect blocks and I/O blocks to communicate with the outside world are the main component of the most of the FPGA devices. In FPGA, the circuits that can be programmed by means of a set of bit streams completely specify the logical functions and connectivity to be implemented. Interconnections are established among various LUTS and they are implemented using multiplexers (MUX). To configure the FPGA to a particular design the CLB's, router and I/O pins are need to be configured. This will be configured by means of a set of bit streams completely specify the logical functions and connectivity which is provided by Xilinx ISE Software. This Software takes the input as HDL Code of particular architecture and generates a set of bit stream to configure particular FPGA. Since FPGA is a programmable hardware device, it is possible to achieve the flexibility of software as well as the speed of hardware at the same time. Hence FPGAs can be viewed as programmable ASICs.

Hence, the FPGAs are expected to offer better performance than the conventional DSP processors for executing different modulation schemes [14]-[16] in real time without loosing the flexibility.

B. Synthesis Results of Some Modulation Schemes

Even though synthesis studies for five different modulation schemes using Verilog codes have been carried out, for the sake of brevity of presentation, only two such schemes viz. the ASK and FSK are presented here. However, result of the synthesis of all 5 schemes singly or combined is depicted in the Table I. The architectures for individual and combined modulation schemes were implemented on Xilinx Vertex IV FPGA. The simulation of individual and composite modulation schemes using matlab simulink blocks is also studied. Both give satisfactory results. HDL synthesis report for ASK and FSK modulation schemes are given below:

1) Synthesis report of ASK modulation

Target Device: xc4vlx25-10-ff6688; Product Version: ISE 9.1i; Speed Grade: -10; # IOs: 40;

#Cell Usage: #BELS: 38 (# GND: 1; # LUT2: 21; # LUT3: 1; # MUXCY: 14; # VCC: 1)#IO Buffers: 40 (# IBUF: 32; # OBUF: 8)#Number of Slices: 12 out of 10752 0% #Number of 4 input LUTs: 22 out of 21504 0%#Number of bonded IOBs: 40 out of 448 8% #Maximum combinational path delay: 8.508ns (6.582ns logic (77.4%), 1.927ns route (22.6%))# CPU: 19.14 /19.27 s | Elapsed: 25.00 / 26.00s.

2) Synthesis report of FSK modulation

Target Device: xc4vlx25-10-ff6688; Product Version: ISE 9.1i; Speed Grade: -10; # IOs : 40;#Cell Usage: # BELS: 24 (# GND: 1; # INV: 2; # LUT1: 1; # LUT2: 1; # LUT3: 8; # LUT4: 3; # MUXCY: 7; # VCC: 1)# IO Buffers: 40 (# IBUF: 32; # OBUF: 8)# Number of Slices: 9 out of 10752 0% # Number of 4 input LUTs: 15 out of 21504 0%# Number of bonded IOBs: 40 out of 448 8% # Maximum combinational path delay: 8.197ns (6.270ns logic (76.5%), 1.927ns route (23.5%))# CPU: 18.59 / 18.73 s | Elapsed: 21.00 / 21.00s.

IV. Architecture of Proposed Reconfigurable Radio Processor

A. Proposed Reconfigurable Architectures

The proposed architecture consists of a number of building blocks for performing the signal processing functions, a number of switches for routing functions and a control unit to generate the control signals for a given scheme.

The architecture combines five different types of modulations functions i.e. AM, ASK, BPSK, QPSK and FSK [14]-[16]. Therefore, all the basic building blocks that are needed for the above mentioned modulation schemes are kept as fixed hardware.

However, the efficiency of the proposed scheme depends on the trade-off between two important factors that are to be determined. They are minimum number of basic building blocks required for combined modulation and the minimum number of switches. To determine these two factors, a new technique **"Common Block Diagram Elimination Method (CBDEM)**" has been adopted which is discussed in the following Section.

B. Common Block Diagram Elimination Method (CBDEM)

Since the proposed architecture combines five different types of modulator i.e. AM, ASK, FSK, BPSK and QPSK, so, the elimination of block diagram is derived. The first step is to find out all the basic building blocks that are needed for all these modulation schemes and then in next step common block is eliminated keeping fix one of block to get minimum number of blocks required in the composite circuit to achieve any of these modulation schemes.

1) Proposed architecture using CBDEM

For the experimental purpose five modulation schemes have been considered. Since the aim of the proposed architecture is to minimize switching delay for configuring a particular modulation. Substantial reduction of hardware for composite modulator is also another aim. For this purpose, CBDEM has been adopted as follows:

Step1: Identifying the all individual blocks from all modulation schemes.

Step2: Drawing the separate block diagram for individual modulation scheme.

Step3: Finding the Precedence relationships among the blocks.

Step4: Combining the two modulation schemes by eliminating the common blocks leaving one such block. This combined two modulation schemes are also combined with another one modulation scheme by elimination of common block. This elimination method is repeated unless all modulation schemes are covered.

A new reconfigurable architecture is developed considering above mentions steps. Fig. 1 depicts the proposed architecture (combined simulink block diagram of the five modulation scheme). This Proposed architecture was synthesized for FPGA technology. HDL (here verilog) was used to represents this proposed architecture. The verilog code for the proposed architecture was synthesized by Xilinx

ISE software for the target FPGA device (Vertex-IV). Synthesizing the verilog code of proposed architecture the Xilinx ISE software produced the schematic view of the proposed architecture and also provides the Floor Planning view of the proposed architecture. The Fig. 2 & Fig. 3 shows the Schematic view and Floor Planning view of the proposed architecture for that FPGA Technology.

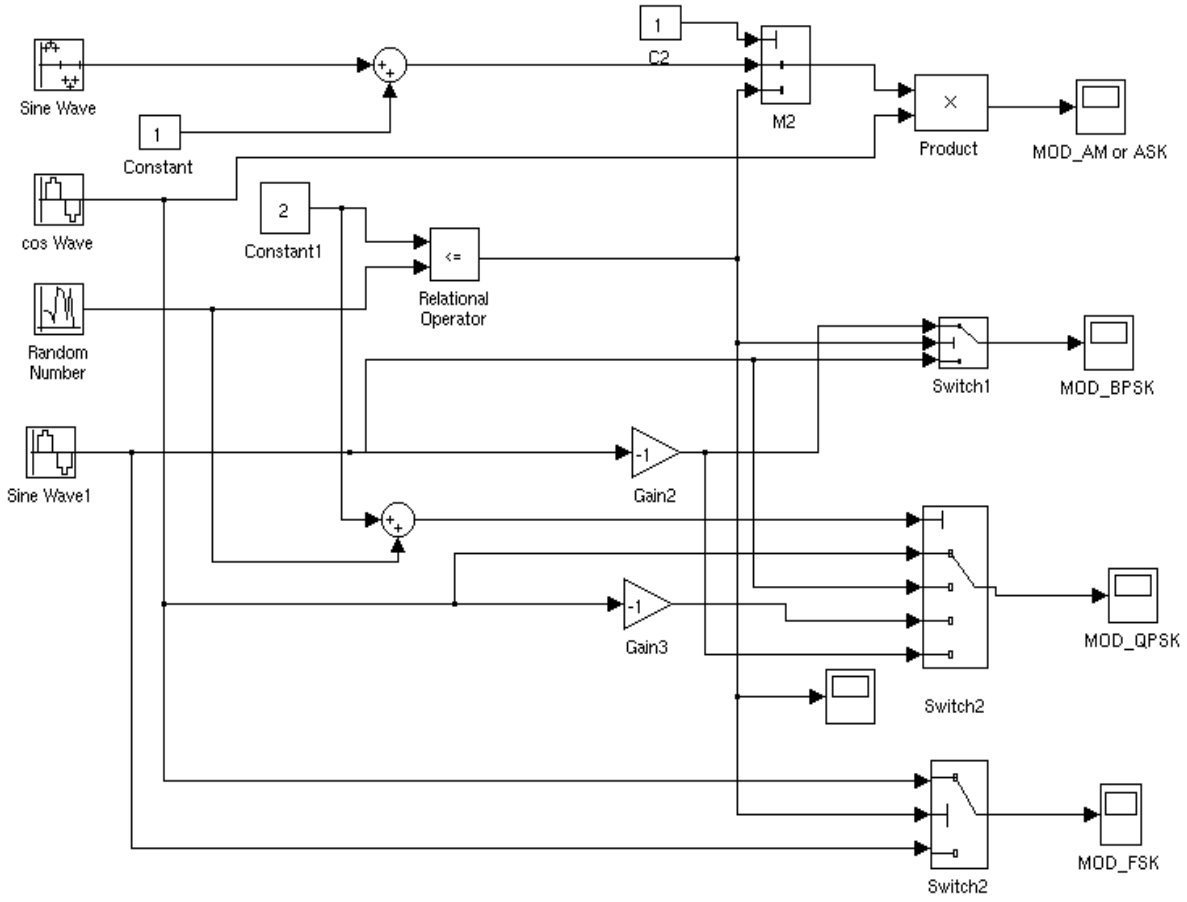

Fig. 1. Simulink model of the proposed architecture (combined five modulation schemes).

Fig. 2. Schematic View of the Proposed Architecture for FPGA Technology.

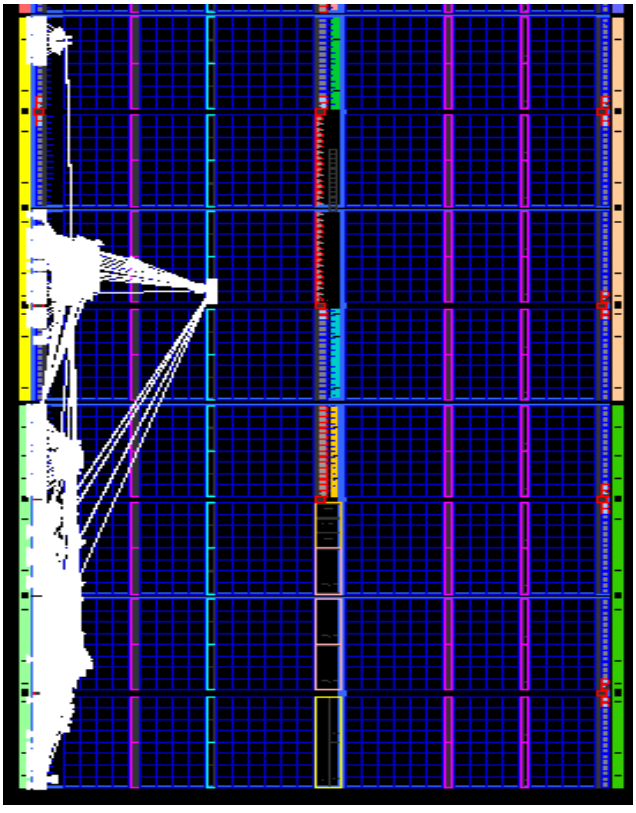

Fig. 3. Floor Planning View of the Proposed Architecture for FPGA Vertex-IV Platform.

The main advantage of the proposed architecture is to perform modulation operation of any of the five modulation schemes by generating different control signals to the Switches/Multiplexers. Thus, the speed of the hardware and flexibility of the software both are achieved. In this context, it is worth noting that even though the proposed architecture offers the hardware speed which is close to ASIC, they can not offer the same level of performance because of routing delay.

To design this proposed architecture, first individual all five modulation schemes are developed by simulink block and simulated successfully. Then following the above described method CBDEM the composite modulator is developed as simulink model depicted in Fig. 1. The individual modulation scheme is simulated from this combined modulator by changing the configuration switches.

Finally a Verilog code of the proposed architecture is developed and synthesized in Xilinx Vertex IV FPGA. The synthesis report of the proposed architecture is given in following section.

C. HDL Synthesis Report of the Proposed Reconfigurable Architectures

Target Device: xc4vlx25-10-ff6688; Product Version: ISE 9.1i; Speed Grade: -10; # IOs: 88;

#Cell Usage: # BELS: 289 (# GND: 1; # INV: 9; # LUT1: 31; # LUT2: 46; # LUT3: 31; # LUT4: 61; # MUXCY: 69; # MUXF5: 3; # VCC: 1; # XORCY: 1);

#IO Buffers: 40 (# IBUF: 32; # OBUF: 8);

#Number of Slices: 91 out of 10752 0%;

#Number of 4 input LUTs: 160 out of 21504 0%;

#Number of bonded IOBs: 88 out of 448 8%;

#Maximum combinational path delay: 17.2508ns (12.833ns logic (74.4%), 4.417ns route (25.6%));

#CPU: 25.09 / 25.22 s | Elapsed: 29.00 / 29.00s.

V. Overall Analysis

From experimental results depicted in the comparison table we can conclude that the hardware like LUTs, Slices, BELS and Bounded IOBs etc. of the combined modulation scheme is reduced due to use of common block diagram elimination method. Other cause of this reduction of hardware of the proposed architecture is that LUTs are replaced by adder, multiplier etc. of the proposed architecture. Since the number of switches is small and the basic building blocks are static, the composite architecture will be able to offer a speed close to ASIC.

TABLE I: The Comparison Table

Modulation Schemes	Different Constraints				
	Combinational Path Delay	**No. slices Used**	**No. of LUT Used**	**Cell usage: BELS**	**Bounded IOB**
AM	21.224ns (17.04ns) logic (80.3%), 4.184ns route (19.7%))	36	64	183	40
ASK	8.508ns (6.582ns logic (77.4%), 1.927ns route (22.6%))	12	22	38	40
BPSK	8.431ns (6.914ns logic (82.0%), 1.517ns route (18.0%))	13	23	40	40
FSK	8.197ns (6.270ns logic (76.5%), 1.927ns route (23.5%))	9	15	24	40
QPSK	12.646ns (6.864ns logic (54.3%), 5.782ns route (45.7%))	31	56	61	40
Proposed Scheme	17.250ns (12.833nslogic (74.4%), 4.417ns route (25.6%))	91	160	289	88

VI. Conclusion

In this paper, feasibility of implementing SDR using the state of the art FPGA is explored and the proposed architecture which combines five modulation schemes was synthesized on Xilinx Vertex-IV FPGA. From experimental results we conclude the following:

1) The various hardware blocks are reduced. So, the greater area within the FPGA is utilized by the combined architecture compare to any single modulation scheme.
2) Compared to dynamic reconfiguration technique for single modulation scheme, our approach eliminates reconfiguration latency when the needed modulation schemes are available in the composite architecture.

FPGAs may not be able to offer the cost effective solution because of their poor silicon utilization factor and high configuration latency at run time. Hence future work may be carried on investigating the cost complexity analysis of the architecture for VLSI implementation on ASICs.

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Amiya Karmakar was born in Kolkata, India and obtained his master of Technology (M.Tech.) in Computer Sc. & Engineering with specialization in Embedded Systems from West Bengal University of Technology in 2005.

Mr. Karmakar has been engaged in teaching and research for the last ten years. He has been working with West Bengal University of Technology, as the project officer for last eight years. Prior to this assignment he was with Polytechnic college at Kolkata as a lecturer (Part time). His areas of research include Embedded System Design, Re-configurable Architecture using FPGAs, Software Defined Radio (SDR), VLSI design, Digital Signal Processing, etc.

Amrita Saha was born in Kolkata, India and obtained her M.Sc. degree in Electronic Science from Kolkata University in 2001 and master of Technology (M.Tech) in Computer Sc. & Engineering with specialization in Embedded Systems from West Bengal University of Technology in 2006.

Ms. Saha has been working in industry and academics for the last twelve years. She is currently working in the Dept. of Electronics & Communication Engineering of Neotia Institute of Engineering & Management (An Instiotute affiliated to West Bengal University of Technology) and is working towards her Ph.D. degree. Her research interests include embedded systems design, special purpose processor design, FPGA based reconfigurable architecture and software defined radio.

Amitabha Sinha was born in Kolkata and obtained Ph.D. degree in Computer Sc.& Engg. from Indian institute of Technology (IIT), Delhi in 1984.

He has been working with Neotia Institute of Technology, an Institution affiliated to West Bengal Univ. Of Technology as a principal. Prior to this assignment, he was with West Bengal University of Technology, Kolkata, India as a professor and director, school of Engg. & Technology since August 2005/2006.

He has more than 25 years of experience in industry, premier academic institutes, R&D centers and IT/Telecom organizations in India & abroad and his areas of research include embedded system design, VLSI design, digital signal processing, re-configurable architecture using FPGAs, software defined radio, processor architecture and system on-chip design, advanced computer architecture, etc.

He was an assistant professor of the Dept. of Comp. Sc.& Engg., Bengal Engineering College (Now Bengal Engineering & Science University), West Bengal, India during 1985-1991 and Associate Professor of the Dept. of Comp. Sc.&Engg, BITS Pilani, during 1997-1998. He was visiting faculty, Dept. of Computer Sc.&Engg., Oakland University, U.S.A. during 1994 and 1999. He was an expatriate faculty member of a premier Malaysian University Mara Institute of Technology during 1994-1995. Prof. Sinha also served R &D centres of different premier industries in the country at senior levels. With an Electronics & Comm. Engineering background, he holds a Ph.D. degree in Computer Sc.& Engg. from Indian institute of Technology (IIT), Delhi which he had obtained in 1984.