

Logic Circuit Design Based on Series-Connected CMOS-NDR Circuit

Kwang-Jow Gan, Zhen-Kai Kao, Cher-Shiung Tsai, Din-Yuen Chan, and Jian-Syong Huang

Abstract—In this paper, we propose a MOS-BJT-NDR circuit, which can show the negative-differential-resistance (NDR) characteristic in its current-voltage (I-V) curve. This NDR circuit is composed of standard Si-based metal-oxide-semiconductor field-effect transistor (MOS) and bipolar junction transistor (BJT). Therefore, we can implement the applications using the standard CMOS process. We demonstrate the design of some logic circuits using the series-connected CMOS-NDR circuit based on the monostable-bistable transition logic element (MOBILE) theory. This logic circuit is designed based on the standard 0.18 μm CMOS process.

Index Terms—CMOS process, logic circuit, monostable-bistable transition logic element (MOBILE), negative-differential-resistance.

I. INTRODUCTION

The negative differential resistance (NDR) devices have attracted a great deal of interest in many analog and digital circuits owing to their unique folded current-voltage (I-V) characteristic and great potential to reduce circuit complexity. The applications using the monostable-bistable transition logic element (MOBILE) has been developed and applied to circuits [1]-[4]. The MOBILE is a functional logic gate with the advantages of multiple inputs and functions where the circuit is made of two series-connected NDR devices and driven by a clocked bias to produce a mono-to-bistable transition.

The previously published MOBILE circuit is made of the resonant tunneling diode (RTD), which requires the III-V process, such as the molecular-beam-epitaxy (MBE) or metal-organic-chemical-vapor-deposition (MOCVD), to fabricate its application. However, the design of the RTD-based applications lack of a reliable or commercial CAD tool. This will limit the development of the RTD-based applications.

The mainstream ULSI technology is still dominated by the CMOS process at present. Recently, our research group demonstrated a novel NDR circuit composed of the Si-based metal-oxide-semiconductor field effect transistors (MOS)

and bipolar junction transistors (BJT), which was named as the MOS-BJT-NDR [5]. The great advantage of this NDR circuit is that we can fabricate their applications using the standard CMOS process. In this paper, we demonstrate the logic circuit designs using this CMOS-NDR-based MOBILE circuit under different controls and input conditions. The simulation is based on the 0.18 μm CMOS process provided by the Taiwan Semiconductor Manufacturing Company (TSMC) foundry.

II. NDR CIRCUIT AND MOBILE OPERATION

The MOS-BJT-NDR circuit used in this work is made of two Si-based MOS and one BJT devices, as shown in Fig. 1(a). By suitably determining the MOS width/length (W/L) parameters, we can obtain the I-V curve with the NDR characteristic. In particular, this NDR circuit possesses the ability to control the peak currents by the external voltage terminal V_{gg} . The V_{gg} value must be large enough to turn on the MN1 and BJT devices. Fig. 1(b) shows the simulated Λ -type I-V characteristics by varying the V_{gg} values with 1.55V, 1.6V, and 1.65V, respectively. The device parameters are designed as $W_{MN1}=10 \mu\text{m}$, $W_{MN2}=10 \mu\text{m}$, and $L_{MN1,2}=0.18 \mu\text{m}$. The BJT uses the standard npn2 cell based on the CMOS process provided by the TSMC foundry. The operation of this NDR circuit had been discussed [5].

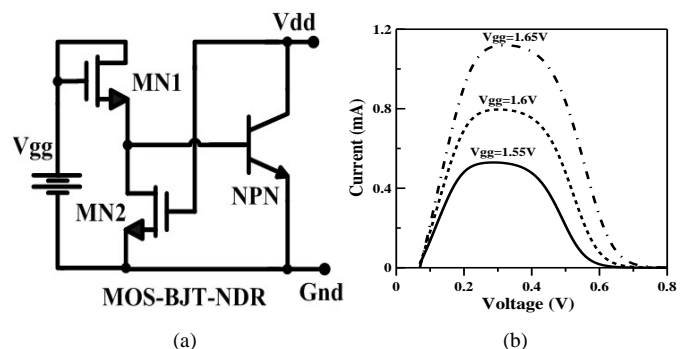


Fig. 1. (a) The circuit configuration of a MOS-BJT-NDR circuit, (b) The I-V characteristics with different V_{gg} values.

The V_{gg} value must be large enough to turn on both the MN1 and BJT devices. As seen, when the V_{gg} is fixed at 1.6 V, the simulated peak voltage (V_p) is 0.3 V, valley voltage (V_v) is 0.7 V, and peak current is 0.8 mA. It should be noticed that the current corresponding to the zero voltage is not zero. It is because the initial operating state for the BJT device is saturated. So there exists a reverse current back to the V_s terminal.

The MOBILE is a functional logic gate with the advantages of multiple inputs and functions where the circuit is made of two series-connected NDR circuits and driven by a

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clocked bias to produce a mono-to-bistable transition. The basic circuit configuration is shown in Fig. 2.

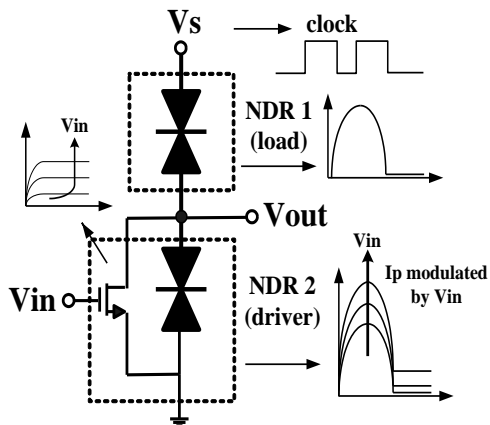


Fig. 2. The configuration of a basic MOBILE circuit.

The upper NDR1 circuit, which is composed of a MOS-BJT-NDR circuit, is considered as the load, and the lower NDR2 circuit, which is composed of a MOS-BJT-NDR circuit in parallel connection with a NMOS device, is regarded as the driver. The supply voltage V_S is a clocked signal. When the clocked bias rises, the voltage at the output node goes to one of two possible stable states (low and high, corresponding to logic “0” and “1”), depending on the relative peak-current magnitude of two NDR circuits. The current of the NDR2 circuit is the sum of the current passing through a MOS-BJT-NDR and a NMOS device. Since the NMOS current can be increased by increasing the V_{in} . Therefore, we can modulate the peak current (I_p) by the magnitude of the input voltage V_{in} .

III. LOGIC CIRCUIT DESIGN

Considering the operation of an inverter, the stable operating point can be determined by the intersection point of two I-V characteristics with the load-line analysis [6], as demonstrated in Fig. 3.

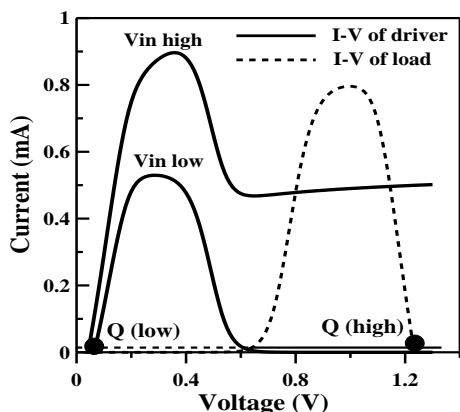


Fig. 3. The load-line analysis for an inverter logic.

The load line, represented by the dashed lines, is the I-V characteristic of the NDR1 device. The I-V characteristic of the NDR2 device is shown by the solid lines. When the bias voltage is smaller than twice the peak voltage, there is only one stable point (monostable) in the series circuit. However when the bias voltage is larger than two peak voltages but smaller than two valley voltages, there will be two possible

stable points (bistable) that respect the low and high states (corresponding to “0” and “1”), respectively. A small difference between the peak currents of the NDR1 and NDR2 devices determines the state of the circuit.

When the input voltage V_{in} is low (logic “0”), if the I_p of driver is smaller than that of load, the circuit switches to the stable point Q corresponding to a high output voltage, as demonstrated by Q(high). On the other hand, if the I_p of driver is bigger than that of load, the circuit switches to the stable point Q corresponding to a low output voltage, as demonstrated by Q(low). Therefore, a small difference of the peak currents between the driver and load could determine the state of the circuit.

The simulated result is shown in Fig. 4. The V_{in} is inputting a square signal with 1.3 V amplitudes. The frequency of the V_S is 50 MHz. The control voltages V_{gg} are designed as 1.6V and 1.5V for NDR1 and NDR2, respectively. As shown, the output switches to the high level if the input voltage is low and switches to the low level as the input voltage is high. The low and high states of V_{out} are about 0.05 V and 1.24 V, respectively.

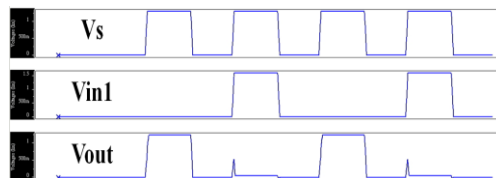


Fig. 4. The simulated result of an inverter operation.

During suitably expanding the MOBILE circuit with multiple-input signals, we can obtain various logic functions. The circuit is shown in Fig. 5. There are eight input gates, V_{in1} and V_{in3} , V_{in2} and V_{in4} , V_{in5} and V_{in6} , and V_{in7} and V_{in8} are used as the input signals for the operation of the AND (or OR), NAND (or NOR), XOR, and XNOR, respectively.

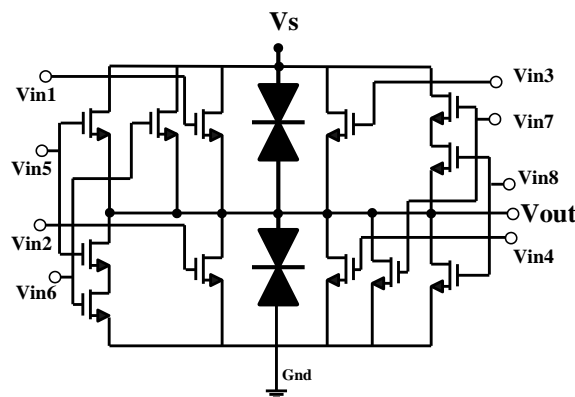


Fig. 5. The MOBILE circuit with multiple-input signals.

The V_{gg} values should be carefully design for different logic function. Considering the operation of the OR gate, two gates V_{in1} and V_{in3} are used as the input signals. The load-line demonstration is shown in Fig. 6.

When both V_{in1} and V_{in3} are at logic “0”, the I_p of the NDR1 circuit is smaller than that of the NDR2 circuit. The stable point will be located at the Q(low), which is corresponding to a low output voltage. With one of the inputs at logic “1” and the other at logic “0”, the I_p of the NDR1 circuit is bigger than that of the NDR2 circuit. Therefore, the

stable point will be switched to the Q(high). When both inputs are at logic “1”, the I_p of the NDR1 circuit is still bigger than that of the NDR2 circuit. Thus the operating point is still located at the Q(high). The control voltages V_{gg} are designed as 1.52 V and 1.55 V for NDR1 and NDR2, respectively. The simulated result is shown in Fig. 7. As seen, the $V_{out}=V_{in1}+V_{in2}$. The design and operation of the AND gate is similar to the analysis of the OR gate. It should be notice that the operating point is determined by the difference of the I_p between the NDR1 and NDR2 circuits.

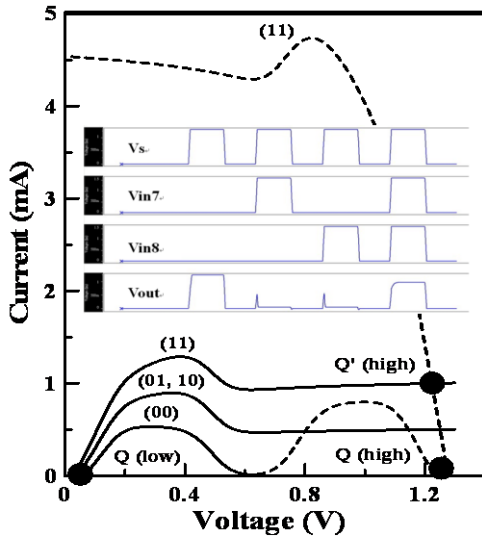


Fig. 6. The load-line analysis for an OR gate operation.

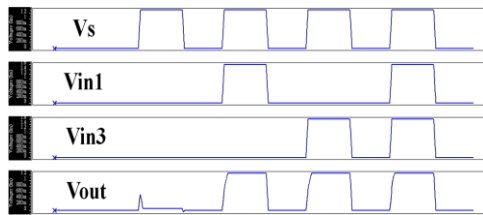


Fig. 7. The simulated result of an OR operation.

Considering the operation of the NAND gate, two gates V_{in2} and V_{in4} are used as the input signals. The load-line demonstration is shown in Fig. 8. When both V_{in2} and V_{in4} are at logic “0”, the I_p of the NDR1 circuit is bigger than that of the NDR2 circuit. The stable point will be located at the Q(high), which is corresponding to a high output voltage.

With one of the inputs at logic “1” and the other at logic “0”, the I_p of the NDR1 circuit is still bigger than that of the NDR2 circuit. The stable point will be located at the Q’(high), which is still remained at the relatively “high” level. When both inputs are at logic “1”, the I_p of the NDR2 circuit is increased and exceeded the I_p of the NDR1 circuit. Thus the operating point will be switched to the Q(low). As seen, the position of the operating points between (00) and (01, 10) states is quite near. They could be recognized with the same high level.

The control voltages V_{gg} are designed as 1.6 V and 1 V for NDR1 and NDR2, respectively. The simulated result is shown in Fig. 9. As seen, the $V_{out}=\overline{V_{in2}}\times V_{in4}$. As for the NOR gate operation, the design and operation is similar to the analysis of the NAND gate.

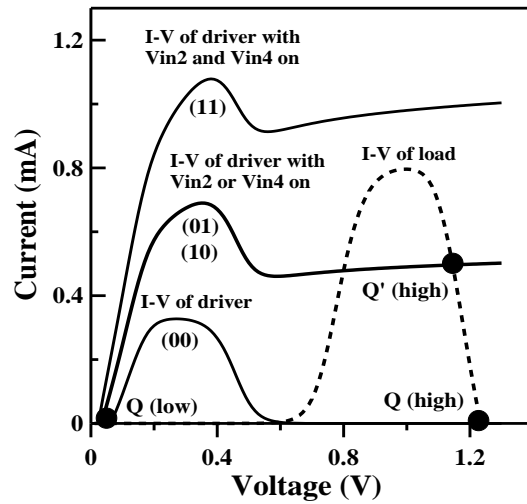


Fig. 8. The load-line analysis for a NAND gate.

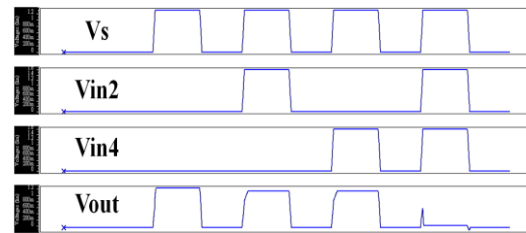


Fig. 9. The simulated result of a NAND operation.

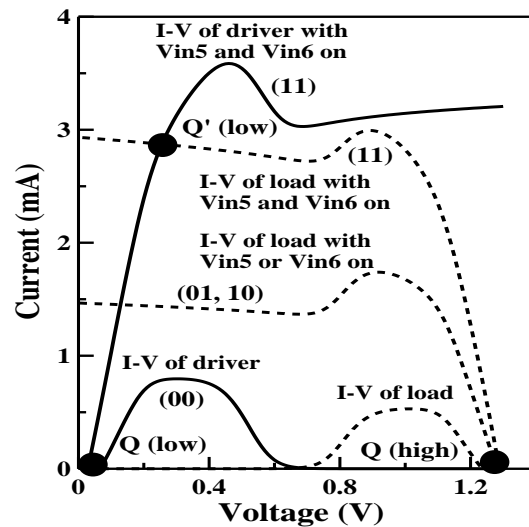


Fig. 10. The load-line analysis for a XOR gate.

The load-line analysis for the operation of an XOR gate is demonstrated in Fig. 10. Here the V_{in5} and V_{in6} are used as the input gates. Firstly, the I_p of the load must be smaller than that of the driver. The operating point will be located at Q(low). When any one of the V_{in5} and V_{in6} is high, the I_p of the load must be bigger than that of the driver. Then the operating point will be located at Q(high). When both V_{in5} and V_{in6} are high, the I_p of the driver should be bigger than that of the load at this moment. Therefore, the operating point will switch to the Q’(low) level, which is corresponding to the relatively “low” level. The HSPICE simulated result is shown in Fig. 11. As seen, the $V_{out}=V_{in5}\oplus V_{in6}$.

Finally, we consider the operation of the XNOR gate. The load-line analysis procedure is similar to the XOR gate

operation, as shown in Fig. 12. Vin7 and Vin8 are used as the input gates. When both Vin7 and Vin8 are at logic "0", the I_p of the NDR1 circuit is bigger than that of the NDR2 circuit. The stable point will be located at the Q(high). With one of the inputs at logic "1" and the other at logic "0", the I_p of the NDR1 circuit is smaller than that of the NDR2 circuit. The stable point will be located at the Q(low). When both inputs are at logic "1", the I_p of the NDR1 circuit is increased and exceeded the I_p of the NDR2 circuit. Thus the operating point will be switched to the Q'(high). The inserted Fig shows the simulated result of this XNOR gate operation. As seen, the $V_{out} = Vin7 \odot Vin8$.

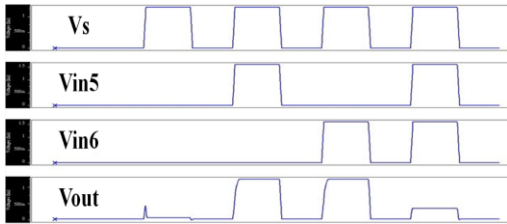


Fig. 11. The simulated result of a XOR operation.

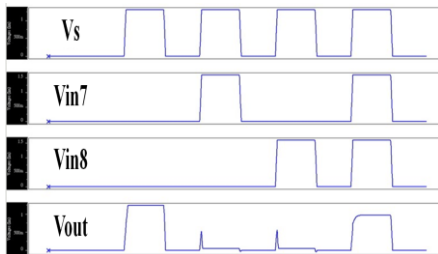


Fig. 12. The load-line analysis and simulated result of a XNOR gate

For the RTD-based MOBILE circuits, they need three series-connected NDR devices to achieve the XOR and XNOR functions [7]-[8]. When the circuit shows the XNOR logic function, the supply voltage V_s will be two times as big as the other logic functions. They also need the MBE system to fabricate the circuit. Compared to them, our design possesses a compact circuit configuration with only using two series-connected NDR circuits. The supply voltage V_s is fixed for all logic functions. Because the whole circuit is composed of the MOS and BJT devices, we can implement its applications using the CMOS technique without the need of a MBE system. The design of this CMOS-NDR MOBILE circuit can be simulated and estimated using the commercial CAD tool like HSPICE. In order to achieve higher speed and frequency characteristics, we can use a further scaled-down and advanced CMOS process in the future.

IV. CONCLUSION

We have demonstrated a MOS-BJT-NDR-based MOBILE circuit in this work. This logic circuit can operate various logic functions, such as inverter, AND, OR, NAND, NOR, XOR, and XNOR, under different conditions. Compared to the RTD-based MOBILE circuit, our circuit has the advantage of fabricating the circuit using the standard CMOS process without the need of a MBE system. Compared to the traditional CMOS logic circuits, our design provide the advantage of implementation of multiple-function logic and threshold gate with a compact circuit configuration. The

results indicate the great potential of this circuit for flexibilities and applications in the future.

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